

Journal of Surface Mount Technology

October – December 2009 Volume 22, Issue 4

Fifteenth Annual Pan Pacific Microelectronics Symposium & Tabletop Exhibition

January 26-28, 2010 Sheraton Kauai Resort Kauai, Hawaii

Do you feel the chill in the air? That means it is time to head to the tropical climate of the Hawaiian Islands to do business. Now is the time to register for the Pan Pacific Microelectronics Symposium & Tabletop Exhibition taking place January 26-28, 2010 at the Sheraton Kauai Resort, on Kauai, Hawaii.

The Pan Pacific promotes international technical interchange and provides a premier forum for networking among microelectronics professionals and business leaders throughout the world.

The conference will feature ten sessions, two keynote speakers, and strong technical papers on topics including packaging, interconnection, assembly, microsystems, nanotechnology, and business issues. This international event provides the ideal environment for conducting business, networking, meeting old friends and making new ones.

For more details on the Pan Pacific, or to take advantage of registration packages, please visit smta.org/panpac or contact the SMTA: Phone: 952-920-7682 Fax: 952-926-1819 Email: smta@smta.org



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Information updated daily... check smta.org for the most current association news.

A publication of the Surface Mount Technology Association

Volume 22, Issue 4, October-December 2009

2009 Hutchins Grant Award Recipient Announced Award presented during the SMTA International Annual Meeting in San Diego

The 2009 recipient, Zhaozhi Li (George), a graduate student in Industrial and Systems Engineering at Auburn University in Auburn, Alabama, has been selected by the SMTA Grant Committee for his project entitled "Design, Processing and Reliability Characterizations of 3D Wafer Level Chip Scale Packaging Technology".

George is a researcher in the area of electronics manufacturing and packaging with his faculty advisor, Dr. John L. Evans. During his tenure at Auburn, he has been involved with several applied research programs through Auburn's Center for Advanced Vehicle Electronics (CAVE). In particular, George worked in printed circuit board qualification for automotive applications, reliability packaging and testing for QFN and μ BGA packages for harsh environments applications, and module level

overmolding reliability and thermal performance for automotive electronics. His main topic toward Ph.D. is the research and development of novel 3D Wafer Level Chip Scale Packaging Technology that leverages the fine pitch flip chip process and high throughput, cost-effective wafer level packaging. George received his MISE degree from Auburn University in 2009 and has a Master of Science in Electrical Engineering from Shanghai Jiao Tong University in China and an undergraduate degree in Electrical Engineering from North China Electric Power University.

The Charles Hutchins Educational Grant, co-

sponsored by the SMTA and Circuits Assembly magazine, was established in memory of past SMTA president, educator, and industry colleague, Dr. Charles Hutchins.

The \$5000 grant has been presented annually since 1998 to a graduate-level student pursuing a degree and working on thesis research in electronic assembly, electronics packaging, or a related field. SMTA would like to thank the individuals, companies, and chapters that donated for

Zhaozhi Li (George)

their generous support.

For more information or to make a donation, please visit the Hutchins Grant page on smta.org or contact SMTA Executive Director JoAnn Stromberg at 952-920-7682 or joann@smt.org.

See page 10 for an article written by David about his SMTA accomplishments.

SMTAI 2010 Call for Papers Abstracts due March 5, 2010 Conference: Oct. 24-28, 2010 Orlando, FL

The call for papers for SMTAI (Oct. 24-28, 2010 Orlando, FL) is now available on the SMTAI web site at smta.org/smtai.

Papers should describe significant results from experiments, emphasize new techniques, and contain technical, economic or appropriate test data. Material should be original, unpublished and non-commercial in nature.

Papers are being solicited for the following categories:

- Emerging Technologies
- Components
- Assembly
- PCB Technology
- Process Control
- Business



There are many benefits to participating. These include making a contribution to our industry by sharing your work., helping to advance the industry and your company as you will be recognized by industry colleagues, discounted conference registration, and \$1,000 cash awards for the best of conference paper, best of proceedings paper, and best international paper.

Please submit your abstract today using the on-line form at: www.smta.org/smtai/call_for_papers.cfm.

It is important to be sure to obtain approval to both write and present your paper prior to submitting an abstract. Once a paper is accepted it is our expectation that you have the approvals required. We'll look forward to hearing from you!



Symposium on Avoiding, Detecting and Preventing Counterfeit Electronic Parts

December 2-3, 2009 University of Maryland College Park, MD

The SMTA and CALCE/University of Maryland are pleased to announce that the 3rd Annual Symposium on Avoiding, Detecting, and Preventing Counterfeit Electronic Parts will be held on December 2-3, 2009 at the University of Maryland. Counterfeit electrical, electronic, and electromechanical (EEE) parts pose a significant threat in the global supply chain. In addition to losses to legitimate producers for the components, equipment failures or malfunctions can present situations that cause mission failures, health and safety concerns and could jeopardize national security.

Topics will cover all aspects of this subject including: identification, mitigation, testing techniques, legal strategy, and policy and procedures from industry and government agencies.

Three half-day tutorials will also be featured:

•Counterfeit Parts Avoidance Training for EEE Parts, by NASA/JPL

•Anti-Counterfeiting: The Powers That Be, by Global Intellectual Property Strategy Center, P.C.

•Material Level Evaluation and Electrical Characterization, by CALCE and Integra Technologies

For more information, contact Melissa Serres Marx (SMTA) at 952-920-7682 or melissa@smta.org or visit the website at smta.org.

SMTA Board Of Directors Election Results Announced

The SMTA is pleased to announce its election results for the Board of Directors for the term that began at SMTA International (October 4-8, 2009).

Jeff Kennedy, Celestica, was elected to Chair the Planning Committee. Roy Starks, Libra Industries, Inc. was re-elected Vice President of Membership. Tom Forsythe, Kyzen Corporation, was re-elected as Vice President of Communications. Denis Barbini, Vitronics-Soltec, was re-elected to the Planning Committee.

Those remaining on the SMTA Board of Directors include: VP Technical Programs, Bill Barthel, Plexus Corp.; VP Communications, Tom Forsythe, Kyzen Corporation; Treasurer, Marie Cole, IBM; and Secretary Dr. Kola Akinade, Scientific-Atlanta. Planning Committee members include: Dr. Denis Barbini, Vitronics-Soltec, Inc; Joe Belmonte, ITM Consulting; Hal Hendrickson, Dage Precision Industries Inc.; Dr. Ning-Cheng Lee, Indium Corporation; and Dr. Laura Turbini, Research in Motion.

The SMTA bids a fond farewell to departing Director Irene Sterian, Celestica. She is congratulated for a job well done and given thanks for the years of dedication to the SMTA.

For more information on the SMTA Board of Directors election results, contact SMTA administrator JoAnn Stromberg: joann@smta.org or 952-920-7682.

Upcoming Exhibitor Opportunities Find an Expo & Tech Forum near you!

Tabletop Expos are a great source for networking and company exposure. Attendee registration is free.

Exhibitor registration is open for the following Expos and Tech Forums:

• Philadelphia Expo - November 17

• SE Asia (Penang) Expo - November 19-20

Make sure to check back as additional tabletop shows are added for 2010.

Contact Leslee Johns, leslee@smta.org or 952-920-7682, for more information or questions regarding any of these opportunities. Find more details and a listing of all exhibitor opportunities at the Exhibitor Opportunities page:

smta.org/education/vendor_days/vendor_days.cfm



Two Keynote Presentations at the Pan Pacific Symposium

January 26-28, 2010

Kauai, Hawaii

Attendees to the Pan Pacific Microelectronics Symposium in January will be privileged to enjoy two keynote presentations from respected industry leaders.

On Tuesday, January 26, 2010, Alan Rae, Ph.D., TPF Enterprises LLC, will outline the current state of commercialization and suggest future trends in his presentation "Nanotechnology is Now Starting to Find Applications in Electronics." Dr. Rae has been associated with the electronics and ceramics industry for over 25 years. He is Director of Research for iNEMI and Leader of the Sustainability and Nanotechnologies Task Group of ISO TC 229. Robert Mertens, Ph.D., IMEC, will present "Solar Cells on Ultra-Thin Silicon" on Wednesday, January 27, 2010. In his presentation, the recent results, obtained with two new techniques to produce ultrathin Si foils, much thinner than 100 micron, will be reviewed. Dr. Mertens is a Senior Fellow at IMEC in Belgium.

Visit the website at www.smta.org/panpac for details and to register. For more information on this program please contact Gayle Jackson at 540-763-2191 or gayle@smta.org.



New Webinar on Reworking Leadless Packages

Methods for Reworking Leadless Packages-LGA, QFNs and More Bob Wetterman and Ray Cirimele, BEST, Inc. Thursday, November 19, 2009, 11am - 12:30pm Eastern

LGAs and QFNs have become increasingly common package types used in many portable products due to their reduced real estate requirements on the PWB. In fact there are many industry marketing trends that point to leadless devices crossing over area array devices in terms of the number of placements in the next few

This webinar is designed for engineers, quality engineering, process developers and repair techs who are faced with reworking these devices. After a review of the device types several different rework methods including the use of a split vision rework system, manual soldering a stencil "bump" method and other variations will be reviewed with process pictures and videos. Industry standard inspection criteria for such devices will also be reviewed.

For more information about webinars contact Ryan Flaherty, 952-920-7682 ryan@smta.org.

To register on-line, please visit:

smta.org/education/presentations/presentations.cfm

South East Asia Technical Conference on Electronics Assembly Technologies

November 18-20, 2009 Equatorial Hotel Penang, Malaysia

years.

The SMTA will launch the "South East Asia Technical Conference on Electronics Assembly Technologies" in Penang, Malaysia on November 18-20, 2009. This program will be the main focus of SMTA's new office in Malaysia for 2009.

The South East Asia Technical Conference on Electronics Assembly Technologies will include a oneday tutorial, and a two-day conference and tabletop exhibition. Conference sessions will cover assembly, components, emerging technologies, harsh environment applications, and PCB technology. Companies participating in the program include Henkel, Indium Corporation, Flextronics, Cookson Electronics, Photo Stencil, Jabil and more...

Exhibit space is still available. If your company does business in South East Asia, including Malaysia, Singapore, and Vietnam, this is the event for you.

Contact SMTA SE Asia Executive Coordinator, Bernie Selva, at Bernie@smta.org to request an application and more information.

SMTA Annual Awards Announced Winners honored at SMTA Annual Meeting at SMTA International

During the Annual Meeting at SMTA International, October 7th at the Town and Country Resort and Convention Center in San Diego, CA, the SMTA honored members who have shown exceptional service to the association and the industry.



The Founder's Award honors individuals who have made exceptional contributions to the industry as well as support and service to the SMTA. This

Dr. Ken Gilleo, ET-Trends (right)

year's award was presented to Dr. Ken Gilleo, ET-Trends.

Ken joined the SMTA in 1990 and was elected by the members to the SMTA Board of Directors from 2002 - 2007. While on the Board of Directors he served on the Planning Committee and also as Vice President Technical for five years. During Ken's time as Vice President Technical Programs he oversaw 32 Academy programs, five Pan Pac events, five Harsh Environment Workshops, five Medical Symposiums, five SMTAIs, two Emerging Technology Conferences, one Telecom Workshop, and additionally created the International-Wafer Level Packaging Conference (IWLPC). Ken's creation of the IWLPC (along with Terry Thompson of Chip Scale Review) was extremely important to the SMTA as it allowed the association to connect with an entirely new audience of potential members.

Additional involvement has included serving on the Awards, Nominating, and Anniversary Committees. He also served as Chairman of the Technical Committee for five years and frequently has taught courses, chaired sessions, and made presentations to SMTA chapters. When one of our members needs to "Ask the Expert", the SMTA staff frequently directs them to Ken. If we question – what's on the horizon for our industry, Ken steps in as our "futurist".

Ken has a Ph.D. in organic chemistry and is a chemist, IP analyst, patent litigation expert, writer and consultant in emerging technologies. He has developed getters, low cost plastic packages, adhesives, underfills, and laser sealing for MEMS and MOEMS, and new products for over 35 years and holds dozens of US patents. His flex products have received three R&D 100 Awards. Ken has authored over 500 papers, presentations and workshops. He has written books on flex, PTF and BGAs. His eighth book, on The Day Niagara Falls Turned Green, is a free web download at ET-Trends.com.And finally, Ken stands above the rest because of his positive, "can do" spirit. He is a positive

influence on people, is humorous, and sincere. As a Board member Ken was 100% dedicated to the success of the SMTA.



The Member of Technical Distinction Award recognizes individuals who have made significant and continuing technical contributions to the SMTA. This year our

Dr. Raiyo Aspandiar, Intel (left)

Awards Committee selected Dr. Raiyomand Aspandiar, Intel Corporation, as the recipient of this prestigious award.

Dr. Aspandiar is a member of the SMTA Technical Committee, has published more than 25 technical papers and is the joint holder of 15 patents in the Electronics Packaging and Manufacturing field. He is a graduate of Stanford University.

Raiyo has been very active in promoting and teaching technical programs for SMTA at local and national events. He was instrumental in the formation of the Portland SMTA Chapter and has generously given his time teaching numerous courses and providing technical presentations at chapter meetings. He continues to give of his time in promoting the programs of the SMTA locally and by presenting papers at SMTA conferences.

Dr. Aspandiar has been with Intel Corporation at the Boards and System Assembly Hillsboro, Oregon facility since 1983. He was part of the team that introduced SMT to Intel. Over the years, he has participated in the development of printed circuit boards and assembly processes for motherboards and mobile modules, which contained a myriad of packages for the Intel microprocessors, chip sets and connectors. Raiyo has also been part of the Lead and Halogen Free Initiative within Intel, whose goal is to remove lead and halogens from Intel's packaging, boards and systems products. Currently, Raiyo is working on solder voids characterization at the BGA package level.



The Excellence in Leadership Award honors SMTA members who stand out as strong leaders in the Association. The 2009 recipient of this award is Kathleen S. Palumbo of Production Analysis and Learning Services LLC.

Kathy Palumbo, PALSERV (left)

NEWS & EVENTS

Kathy Palumbo is currently serving as President of the award winning LA/Orange County Chapter. Prior to being elected as President she served as the Secretary of the chapter for six years. During her volunteer time for the chapter her passion was in the designing of both the chapter Web site and chapter newsletter, continually polishing and adding new features so that the chapter "look" and information are current and to ensure that colleagues who came to the chapter Web page would be engaged, become involved and support chapter events.

Kathy makes serving as President look easy; however, everyone knows there is a great deal of time and effort placed on being an organized leader of a highly successful SMTA Chapter. She creates an exciting and professional image of the LA/Orange County Chapter at meetings and in communications to industry colleagues.



Michael Yuk Fai Wong, of Emerson, Hong Kong, has been chosen receive the to 2009 Excellence International in Leadership Award for his continuous commitment to SMTA with regard the SMTA's to

Abby Tsoi (left) accepted for Michael Wong, Emerson

international focus.

Michael Wong has worked in SMT Industry for 20 years and is currently Director of Manufacturing Engineering of Emerson Network Power - Embedded Computing and Power, for the engineering of Emerson factories in China and Vietnam. In 2004 Michael joined the SMTA Hong Kong Chapter as Vice President Technology. Also, he was appointed as the Chair of Technical Advisory Council of SMTA China since its establishment in 2006. He was the pioneer in organizing the "SMTA China Conferences" in Shanghai, Shenzhen and Tianjin in conjunction with Nepcon China events every year. These conferences have become the strongest asset of SMTA China and help to build a very good reputation and a sound technical status of SMTA in China.

Michael has provided outstanding leadership in the Council and SMTA China, insuring the success of SMTA China. He is also one of the Chinese speaking instructors for the SMTA Engineer Certification Program.

Without Michael's excellent leadership and contributions, SMTA China would not be as strong and successful as it is. It is a great pleasure to honor Michael Wong today by presenting him the 2009 SMTA International Leadership Award.



The SMTA Awards Committee unveiled a special award to recognize a colleague who has made an exceptional contribution to the SMTA. The 2009 **Exceptional** Contribution to SMTA award is being presented to Steve Gold of EMS007.

Steve Gold, EMS007 (right)

The EMS007 team has literally revolutionized the concept of media performance, and organizational support, within the SMTA by taking us into the internet video era.

Steve and the EMS007 staff actively and aggressively exhibit at, and report on, SMTA's events. Their video coverage provides rich insight into, and information on, key people, products, processes, and technical advancements in our industry. Steve Gold is found covering technology forecast events, white paper presentations, keynote presentations, and social events for the SMTA across the globe. From Shanghai to Orange County, from a member assembly line to an SMTA golf outing, Steve's presence is felt.

In addition to providing truly groundbreaking new media coverage of our programs, Steve also volunteers on the SMTA MarCom Committee. His diligent participation has helped form many of our most progressive ideas and assisted the Committee in making them a reality.

In 2008, Steve travelled extensively, interviewing some of our industry's leading authorities, to create compelling third-party endorsement interviews for the SMTA 25th Anniversary project. Having located the subjects, secured the rights to the testimonials, and conducted the interviews, Steve then reviewed, edited, and mixed the video into a transformational product that revolutionized the way the SMTA talks to existing and potential new members. Steve worked closely with the SMTA MarCom team, soliciting feedback and enhancements to ultimately craft a finished product that far exceeded the SMTA Membership Committee's goals.

Steve directly and conclusively addresses every single criteria related to excellence in service to the SMTA. And through his dedicated efforts, Steve makes the SMTA a stronger and better organization. For all of this, Steve Gold has clearly earned special recognition for his exceptional contribution.

continued on next page ...

NEWS & EVENTS



Scott Priore for Cisco (center)

The SMTA+ Corporate Partnership Award recognizes а corporate member of the SMTA that has shown exceptional support to the SMTA. We are honored to recognize and present the

2009 SMTA+ Corporate Partnership Award to Cisco Systems Inc.

Cisco Systems Inc. joined the SMTA as a Corporate Member in 2004 and has 33 employee members. Cisco has been a valued supporter of our educational programming by giving presentations, chairing sessions or serving on technical committees on a total of 46 occasions. They have registered over 100 colleagues for SMTA conferences over the years and supported two local chapter officers and one national Board member.

It is with great pleasure that we recognize a company that has gone above and beyond in the support of the SMTA. Congratulations to Cisco Systems Inc. for receiving the SMTA+ Corporate Partnership Award 2009. The Chapter of the Year Award recognizes SMTA Chapters that have shown exemplary commitment to our objective..."Sharing the Knowledge". The overall rating of each chapter is measured in the following areas: membership growth, regular meeting scheduling, timely reporting and communications, creative and informative technical programming, special projects, support of students and student chapters, contributions to the industry and community and volunteer service on SMTA committees.

We are proud to honor four chapters to receive the 2009 Chapter of the Year Award. We recognize the LA/Orange County Chapter, Oregon Chapter, Space Coast Chapter and the Penang Chapter (International Chapter of the Year). The LA/Orange County Chapter has won this prestigious award seven times, the Oregon Chapter has taken home the award five times, and this is the first year the Space Coast Chapter and Penang Chapters have "risen to the top". Congratulations to all four outstanding chapters and their leaders who have been overwhelmingly committed to serving the industry colleagues in their area.



Space Coast Chapter



Oregon Chapter



LA / Orange County Chapter



Penang Chapter

SMTA Conference Excellence Awards Announced

Winners honored at SMTA Annual Meeting at SMTA International

SMTA International offers three recognition awards for contributions to the conference technical program. Award winners receive \$1,000 plus a recognition plaque. The awards are presented each year at the Opening Ceremony. The winning papers are available in the 2008 SMTAI Proceedings or the Knowledge Base at smta.org/knowledge/knowledge.cfm.

"Best of Conference" Presentation

Conference attendees voted that Greg Henshall, Hewlett Packard; Robert Healey and Ranjit S. Pandher, Ph.D., Cookson Electronics; Keith Sweatman and Keith Howell, Nihon Superior Co., Ltd.; Richard Coyle, Ph.D., Alcatel-Lucent; Thilo Sack and Polina Snugovsky, Ph.D., Celestica Inc.; Stephen Tisdale and Fay Hua, Ph.D., Intel Corporation; receive the 2008 Best of Conference award for their presentation entitled "iNEMI Pb-Free Alloy Alternatives Project Report: State of the Industry" The award is based on the conference attendees' rating of each speaker at the technical session. This paper provides the results of an iNEMI study of the present state of industry knowledge on Sn-Ag-Cu alloy "alternatives," including an assessment of existing knowledge and critical gaps. Focus areas are recommended for closing these gaps, with the additional goal of avoiding repeated investigations into issues already resolved. Finally, efforts to update industry standards to account for the new alloys and to better manage supply chain complexity and risk are described.

Dr. Henshall received his Ph.D. in Materials Science from Stanford University in 1987, and then worked as a staff scientist at Lawrence Livermore National Laboratory until he joined Hewlett-Packard in 1996. At HP, Greg has focused on electronic interconnect reliability, and has spent the past nine years working on electronics manufacturing and materials issues related to the lead-free transition. Greg represents HP on the JEDEC JC14 Quality & Reliability committee, and is involved with a number of industry standards groups and consortia, including iNEMI, where he chairs the Pb-Free Alloy Characterization Project.

Greg Henshall, Hewlett

Packard (right)

Pradeep Lall, Ph.D., Auburn University

"Best of Proceedings" Paper

As selected by the SMTA International Technical Program Committee, the paper "Survivability Assessment of SAC Lead-Free Packaging Under Shock and Vibration Using Optical High-Speed Imaging" by Pradeep Lall, Ph.D., Deepti Iyengar, Sandeep Shantaram, Dhananjay Panchagade, and Jeff Suhling, Auburn University, was the 2008 Best of Proceedings paper. This paper discusses methodology for determining survivability of ball-grid array packaging under shock and vibration which has been developed using optical measurements based on digital image correlation (DIC) in conjunction with ultra high-speed imaging. Full-field transient strains have been measured on various board assemblies subjected to shock in various orientations.

Pradeep Lall is the Thomas Walter Professor with the Department of Mechanical Engineering and Associate Director of NSF Center for Advanced Vehicle Electronics at Auburn University. He received the MS and Ph.D. degrees from the University of Maryland and the M.B.A. from Kellogg School of Management. Dr. Lall has ten years of industry experience. He has published extensively in the area of electronic packaging with emphasis on modeling and predictive techniques. He holds several U.S.-patents and is an Associate Editor for the ASME-JEP, IEEE Transactions TCPT, and TEPM.

"Best International Paper"

The paper "Implementation of Increased Cu Levels (1%) in SAC Alloys for PBGA Applications," by



Isabel de Sousa, Donald W. Henderson, Luc Patry, and Robert Martel, IBM Corporation, was selected as the 2008 Best International Paper. The paper describes the effect of altering the basic solder composition of SAC alloy, by adding Cu, to improve the overall soldering process of PBGA with Cu

Marie Cole (right) accepted for Isabel de Sousa, IBM

pads. Detailed solder characterization was described and insight on certain soldering parameters such as base metal dissolution, interfacial reactions and post reflow composition of the solder were given. The core of the paper discusses the reliability behavior of the SAC310 solder composition.

Isabel de Sousa has a M.Sc.A in metallurgy from Ecole Polytechnique of Montreal. She has worked with IBM for 18 years occupying positions of failure analyst at IBM Bromont's manufacturing facility, process engineer for CCGA and in more recent years performed development work for Pb free processes for CGA and BGA.

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JOB LISTINGS

For further information about these ads or to place an ad, contact SMTA director of communications Ryan Flaherty at 952-920-7682 or ryan@smta.org.

All listings are made by SMTA members.

The Job Listings page of the SMTAnews section on smta. org contains updated listings as well as additional contact information. Job lsitings are FREE for members of the SMTA.

POSITIONS AVAILABLE

Incoming Test Technician

SUMMARY DESCRIPTION: Under direct supervision, performs tests of purchased components and assemblies for compliance to specifications; maintains records, logs, and appropriate documentation. Person will work from engineering drawings, electrical schematics, sketches, written/verbal instructions. Responsibilities will include performing assembly work that requires the use of protective equipment (suit, goggles).

EDUCATION: Associate Electronic Technical Certification or education/experience equivalent.

EXPERIENCE: 3 - 5 years of electronic test and troubleshooting experience in manufacturing technology environment in addition to demonstrated inspection/quality experience.

KNOWLEDGE & SKILLS: Must be detail oriented, good manual dexterity, math skills and ability to distinguish colors. Must possess intermediate computer skills. Knowledge and experience in use of mechanical and electronic measurement/ test equipment required and ability to read engineering drawings required. Working knowledge of production and quality processes, procedures and product flow. Must thoroughly understand all testing techniques and instruments.

CONTACT: Interested parties may submit their resume to hrjobs@micromeritics.com, or visit our website www. micromeritics.com. Please be sure to include your pay requirements/history. No phone calls accepted.

SMT Process Technician - Chicago, IL

Prototype shop in Chicago suburbs seeks SMT process technician with 2-4 years of experience. Candidate should have knowledge of entire manufacturing process and have good soldering skills. MYDATA pick and place as well as profiling experience highly desirous. Projects are shepherded from parts knitting all the way through test. There is lots of variety in this job.

Company offers medical, dental, 401K and insurance benefits.

Send resumes to bwet@sbcglobal.net

ICP Process Engineering Manager - Santa Clara, CA

This manager of this approx. 3 person department will be responsible for overseeing development of assembly processes for new programs, sustaining existing processes, defining equipment requirements, reviewing specifications for processes, selecting components, materials and methods to package IC's from wafer to finished product. This manager will review product requirements to ensure compatibility with the available processing methods and will recommend and prepare changes, additions, and modifications to facilitate manufacturing.

Requirements:

BS in Engineering, or equivalent, plus 10+ years in a high tech manufacturing environment, ideally in a semiconductor industry.

Knowledge of semiconductor backend operations required. A record of successful project completion is a must.

A high energy, act quickly attitude is essential.

Able to manage multiple projects, both long term, and short term, simultaneously.

Management/Supervision experience.

Candidate will be active in understanding industry trends and technology by participating in affiliated organizations such as IMAPS, MEPTEC, OSA, IPC or IEEE.

For consideration, remit your resume to yesquer@promex-ind. com. You can learn more about us at our web site, www. promex-ind.com.

Director of Corporate Quality - St. Louis, MO

The Director of Corporate Quality will be responsible for planning, directing and implementing quality policies, programs, and initiatives for LaBarge, Inc.

Essential Functions:

Works closely with the VP's of Operations, Director of Supply Chain, Director of Information Systems and Technology, Directors of Operational Excellence, General Managers and Quality Managers to align our quality initiatives and processes with the overall business strategy.

Analyzes, evaluates and presents information concerning factors such as production capabilities and manufacturing problems for consideration by other members of management team.

Suggests and debates alternative methods and procedures in solving problems and meeting changing market opportunities. Cooperates with other top management personnel in formulating and establishing quality policies, procedures and goals.

Coordinates quality objectives and goals with our production procedures to maximize product quality and minimize costs.

Champion Quality Maturity Assessment and Six Sigma tools and programs and support Lean and 5S initiatives. Serves as our company's representative for any quality certification systems and is responsible for administrating such systems to assure accurate compliance. Interfaces with ISO, QS and FAA as required to maintain a positive working relationship. To apply online visit us at: http://tinyurl.com/LBquality

POSITIONS WANTED

Business-minded Engineer

I am a Ph.D. candidate in Materials Science at the University of Rochester, and currently seeking a full time position in research. With two master degrees and one coming Ph.D. degree, I had extensive research experience in metals, alloys, heat-treatment, material processing, electronic packaging, lead free solder, etc. My thesis research involved experimentation, calculations, FEA simulation and modeling in electronic materials and devices and Matlab programming. With such a thorough training and background I am well prepared for working for your company.

Besides scientific research, I was also a business owner. I helped a French company to start a new business in China by searching suppliers, selecting manufacturers, coordinating between suppliers and customers, checking samples, controlling quality, negotiating price, setting up contracts, and exporting final products to France. With two years of working experience, I gained both business and real industry experience, especially in negotiation and trouble-shooting.

Please view my resume here: http://smta.org/files/Jing_Cheng_Resume.pdf

Engineering & Technical Management

Innovative Engineering Manager with over 20 years of experience in progressively more responsible positions with a variety of electronic industries, combining vision, technical prowess and leadership expertise. Inspired by the complex and never been done before technology challenges to further product performance and development. A proven track record in utilizing creative approaches to process and product design development - demonstrated by numerous U.S. patents and over 35 publications. Problem solver with outstanding analytical skills; strategic thinker; excellent communicator at multiple levels; technical leader with keen vision.

Please view my resume here: http://www.smta.org/files/Lathop_Richard_5-28-09.pdf



Copyright Year : 2007 Non-Member Price : \$169.00 Member Price : \$159.00

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Copyright Year : 2009 Non-Member Price : \$160.00 Member Price : \$150.00

Solder Joint Technology Materials, Properties, and Reliability

King-Ning Tu

Solder joints are ubiquitous in electronic consumer products. With the European Union's directive to ban the use of lead-based (Pb) solders in these products, there is an urgent need for research on solder joint behavior under various driving forces in electronic manufacturing, and for development of lead-free solders. For example, spontaneous Sn whisker growth and electromigration induced failure in solder joints are serious issues. These reliability issues are quite complicated due to the combined effect of electrical, mechanical, chemical, and thermal forces on solder joints. To improve solder joint reliability, the science of solder joint behavior under various driving forces must be understood. This book offers a thorough examination of advanced materials reliability issues related to copper-tin reaction and electromigration in solder joints, and presents methods for preventing common reliablity problems.

SMTA International Conference Proceedings on CD, 2009

This is your reference source for electronics assembly, lead-free, SMT, RFID, process control, flip chip, chip scale, BGA, RoHS compliance, automotive, and more... you'll find the electronic interconnection solutions you need, because this proceedings is dedicated to surface mount, advanced packaging, and related technologies and business operations.

The CD contains the papers from the AIMS Harsh Environment Electronics Workshop as well.



Copyright Year : 2009 Non-Member Price : \$139.00 Member Price : \$129.00

Materials for Advanced Packaging

Daniel Lu and C.P. Wong

Significant progress has been made in advanced packaging in recent years. Several new packaging techniques have been developed and new packaging materials have been introduced. Materials for Advanced Packaging provides a comprehensive review on the most recent developments in advanced packaging technologies including emerging technologies such as 3 dimensional (3D), nanopackaging, and biomedical packaging with a focus on materials and processing aspects.

MEMBER NEWS

SMTA was saddened to learn of the death of former-member **Barry O'Brien** of Horizon Sales and the SMTA Ohio Valley Chapter. Barry covered the Ohio territory for Horizon Sales. In this role, he was instrumental in opening new accounts for Juki Automation Systems, Seika Machinery, Indium Corporation and many other key companies. He was an active participant in the Ohio Valley Chapter and has been a member of SMTA since 1987. Barry had many friends in the industry and will be sorely missed.

Sheldon Brennan, ZESTRON, was promoted to National Sales Manager. Sheldon was actively involved in multiple SMTA projects to support local chapters. In his role, Mr. Brennan will be responsible for growing ZESTRON's domestic product and service business while expanding the current customer base.

Asymtech promoted **Paul Gallo** to Sales Manager, USA and Americas.

Upcoming Events

November 19, 2009

New Webinar: Methods for Reworking Leadless Packages LGA, QFNs and More Bob Wetterman, BEST, and Ray Cirimele, Business Electronics Soldering Technologies, Inc.

November 18-20, 2009

South East Asia Technical Conference on Electronics Assembly Technologies Equatorial Hotel Penang, Malaysia

December 2-3, 2009 Symposium on Avoiding, Detecting and Preventing Counterfeit Electronic Parts University of Maryland College Park, MD

January 26-28, 2010 Pan Pacific Microelectronics Symposium & Tabletop Exhibition Kauai, Hawaii

Visit the SMTA Calendar on the smta web site, smta.org, for more information on the events listed above.

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A Student Connects at SMTA International

My name is David Lau. I would like to thank the SMTA chapters who sponsored my travel to SMTAI in San Diego: Toronto, Atlanta, Space Coast, and Long Island chapters. Without their support I would not be able to have had this valuable experience of presenting my paper. I have met so many great industry people at the conference from around the world. I have also learned a great deal about both the technological and business aspects of the electronics industry by attending the workshops and technical sessions. Finally, I would like to thank my industrial supervisor Dr. Laura Turbini, for her time, guidance, and support as well as all the RIM staff who have taught me so much.

I am also the founding president of the University of Waterloo SMTA student chapter. Our chapter started with 5 graduate students and a professor in the Mechanical Engineering department. We have promoted our chapter to other engineering students by sending out a presentation about the benefits of membership and putting up posters on campus. Our chapter officers have also organized activities including a lab tour at Research in Motion, and have assisted in a workshop held by Struers and the SMTA Toronto chapter. We have successfully recruited undergraduate students from different engineering departments and there are now 18 active members in our chapter.

I am a Master student at the University of Waterloo majoring in Mechanical Engineering. I am funded through an Industrial Postgraduate Scholarship (IPS) from the Natural Science and Engineering Research Council of Canada (NSERC) and Research in Motion where I spent 2 days/ week at the Materials Interconnect Lab working on my research project. My thesis topic is on evaluating halogen-free laminates used in handheld electronic devices. I have correlated the thermal and mechanical properties of halogen-free laminates, which are important to the manufacturing processes and product reliability. Some of these topics were covered in the paper I presented at SMTAI.

If your chapter would be interested in sponsoring a student to attend an upcoming SMTA event, contact Student Chapter Coordinator, Karen Bergseth at 952-920-7682 or karen@smta.org.

smta.org/chapters/student_chapters.cfm

SMTA CHAPTER NEWS

If you are interested in serving

as a chapter officer in your local area, contact SMTA

director of chapter relations Gayle Jackson: gayle@smta.

org or 540-763-2191.

HOT TOPICS

Tennessee Valley (Huntsville) Chapter

The November Chapter Meeting will be held on November 5th 2009 5pm-7pm at Adtran. Denis Barbini, Vitronics Soltec, will be the speaker for the program. Featured topics are Solder Processes, Pb-Free Solder and DFM.

Silicon Valley (San Jose) Chapter Chapter Meeting/Holiday Party Thursday, Nov 12, 2009

Tampa Bay Chapter

Chapter Meeting

Christian Ott, SEHO Systems GmbH, will present a paper titled "Effects of an Appropriate PCB Layout and Soldering Nozzle Design on Quality and Cost Structure in Selective Soldering Processes." Tampa, Florida Wednesday, November 18 2009

Arizona-Sonora Chapter

Lunch Meeting November 18, 2009, 11:30 am Fiesta Resort, Tempe, AZ

Oregon Chapter

Chapter Meeting - "Failure Analysis" November 18, 2009

Atlanta Chapter Chapter Meeting November 19, 2009

LA-Orange County Chapter

Presentation Dinner Meeting Design - The Key to Cleaning, Defluxing and Productivity Barbara Kanegsberg, BFK Solutions, LLC Thursday, November 19th, 2009

Dallas Chapter

Luncheon Roundtable Discussions Lunch and Group Discussions begin at 11:30 am Dave and Buster's Dallas, Texas December 03, 2009

Dallas Chapter Chapter Tutorial Program "Lean and Green" by Phil Zarrow, ITM

January 19, 2010

LA-Orange County Chapter Chapter Tutorial Program "Lean and Green" by Phil Zarrow, ITM January 21, 2010

ON TOUR

Upper Mid-West Chapter Chapter Meeting and Tour November 3rd, 2009 "Counterfeit Components" by Phil Zarrow, ITM Tour: General Dynamics Bloomington, MN

Indiana Chapter

Chapter Meeting and Tour Tour the PCB shop and Battery Division of Naval Surface Warfare Center - Crane Division Presentations on Embedded Passives and Overmold of Electronics Modules with Novel PCB Lamination Crane, Indiana November 19th, 2009

FUN AND GAMES

Space Coast (Melbourne FL) Chapter Expo and Barbeque FREE BBQ LUNCH FOR ALL ATTENDEES Wednesday, November 4th, 2009 10:00 am to 3:00 pm Lagoon House Education Center Palm Bay, FL

Empire (NY) Chapter SMTA 25th Anniversary Celebration and Meeting 12:00pm

SHOW TIME

Wisconsin Chapter Wisconsin Expo & Tech Forum November 10, 2009 Wyndham Airport Hotel Milwaukee, WI

Philadelphia Chapter

Philadelphia Expo & Tech Forum November 17, 2009 Radisson Hotel Valley Forge King of Prussia, PA

Penang SE Asia Chapter

Technical Conference on Electronics Assembly Technologies and Tabletop Expo November 19-20, 2009 Equatorial Hotel Penang, Malaysia

Attendee registration is FREE for Expos and Tech Forums! Plan to attend now and visit with representatives from the major suppliers to the industry, have a chance to win great door prizes, attend **free** technical sessions, and enjoy a **free** lunch! Pre-register to ensure your **free** lunch! For more information please contact Leslee at 952-920-7682, leslee@smta.org.



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— Srini Chada, Ph.D.

The Journal of SMT Editor/Journal Committee Chair

EVALUATION OF LEAD-FREE SOLDERS, HALOGEN-FREE LAMINATES, AND NANOMATERIAL SURFACE FINISHES FOR ASSEMBLY OF PRINTED CIRCUIT BOARDS FOR HIGH RELIABILITY APPLICATIONS

Gregory Morose¹, Sammy Shina², Robert Farrell³, Michael Ellenbecker², and Rafael Moure-Eraso²

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ABSTRACT

There has been a global effort in the electronics industry recently to adopt green materials for the production of printed circuit boards (PCB's). However, there are technical and economic challenges that remain to hinder the universal implementation of green materials, especially for high reliability electronics applications.

The research presented in this paper was conducted by the members of the New England Lead-free Electronics Consortium. The objective was to evaluate the solder joints of electronics assemblies produced with various lead-free, halogen-free, and nano materials for use in high reliability applications. The test vehicle was 0.110" thick and densely populated with various components, which greatly increases the assembly challenge and differentiates this research from industry work with thinner, less populated test vehicles. Visual inspection procedures for this research meet IPC Class 3 standards for High Performance Electronics Products. This Class 3 standard is utilized for inspecting electronics assemblies used for high reliability applications. The lead-free materials that were evaluated during the assembly included four PCB surface finishes, two through hole technology (THT) solders, and three different surface mount technology (SMT) solder pastes. The results of the lead-free assemblies were compared against baseline data obtained by assembling similar test vehicles using tin/lead materials.

The assembly of lead-free electronics for high reliability applications is achievable with equal or less solder joint defects than tin/lead assemblies. This is viable with the careful selection of both lead-free solder and surface finish materials.

Key Words: Lead-Free, Halogen-Free, Nanomaterials, Printed Circuit Boards, RoHS, DoE

INTRODUCTION

The major types of drivers for moving manufacturers towards lead-free electronics include regulatory and market drivers. The major regulatory driver has been the European Union's Restriction on the use of certain Hazardous Substances (RoHS) Directive that was enacted in 2003. This directive limits the amount of lead and five other substances that are used in electrical and electronic equipment. These amounts are listed in Table 1 below. The RoHS directive covers some, but not all, electrical and electronic equipment placed on the European Union market as of July 2006. There are several types of electronics products that are either exempt or considered out of scope from this directive. This includes electronics products requiring high reliability such as network infrastructure, aerospace, defense, and medical applications [1]. These high reliability applications are the focus of this research. Because of these exemptions, there is continued use of lead in the electronics industry for many products sold in the European Union. [2]

Substance	Maximum Concentration
Lead	< 1,000 ppm
Mercury	< 1,000 ppm
Cadmium	< 100 ppm
Hexavalent Chromium	< 1,000 ppm
Polybrominated biphenyls	< 1,000 ppm
Polybrominated diphenyl	< 1,000 ppm
ethers	

Table 1: RoHS Directive Maximum Concentrations

The objective of this research was to evaluate the solder joints of electronics assemblies produced with various lead-free and halogenfree materials for use in high reliability applications. The defect level of the lead-free assemblies was compared to the tin/lead assemblies. Visual inspection procedures for this research meet IPC-A-610 Class 3 standards for High Performance Electronics Products. This Class 3 standard is used for inspecting electronics assemblies used for high reliability applications. For lead-free electronics, it is desirable to be able to assemble PCBs with lead-free solder joints that have equal or less defects than PCBs assembled with tin/lead solder. Subsequent research by the Consortium will be conducted in the future to further evaluate the long-term reliability of these test vehicles by using accelerated testing techniques.

Experimental Procedure

The assembly of 35 test vehicles occurred during 2008 at the Benchmark Electronics facilities in Hudson, New Hampshire and Guadalajara, Mexico. The test vehicle shown in Figure 1 is eight inches wide by ten inches long, contains 20 layers, is 0.110 inches thick, and is densely populated on both sides with SMT and THT components. The test vehicle included a number of thermally disparate Surface Mount Technology (SMT) components which made assembly challenging. The results are applicable for similar sized PCBs and can be extrapolated to thinner, less thermally disparate PCBs which are more common in the electronics industry.



Figure 1: Assembled Test Vehicle

There were 886 SMT components (BGAs, microBGAs, resistors, TSOPs, PQFPs, PQFN, and MLFs), and 21 THT components (connectors, LEDs, DC/DC convertors, and capacitors) assembled on each test vehicle. Table 2 provides the component counts for the total amount of SMT and THT components used for the assembly of the test vehicles.

Com- ponent Type	Compo- nents Per Board	Lead- free DOE (24 test vehicles)	Tin/Lead DOE (8 test vehicles)	Halogen- free (3 test vehicles)
Surface mount	886	21,264	7,088	2,658
Through hole	21	504	168	63
Totals	907	21,768	7,256	2,721

Table 2: Component Counts for Test Vehicle Assembly

This research included four different PCB surface finishes.

1. Electroless Nickel Immersion Gold (ENIG). This surface finish involves using both electroless and immersion technologies to deposit the metallic surface finish.

2. Hot Air Solder Leveling (HASL). For this research, the surface finish used the lead-free alloy Sn100C that is comprised of mostly tin, but also includes 0.6% copper, 0.05% nickel, and 0.0055% germanium.

3. Organic Solderability Preservatives (OSP).

4. Nano materials surface finish using nanosilver particles dispersed in a polymer (polyaniline), with a thickness between 45 to 65 nm. This was selected because it is a new finish and has the potential of addressing major lead free implementation challenges such as copper dissolution during rework and process improvement for assembly of lead-free THT components. Moreover, this finish uses significantly less silver as compared with a standard (non-nanotechnology based) silver finishes and is applied at lower temperatures which makes it environmentally more friendly and less thermally stressful to the PCB.

This research included the following three different solder pastes for assembly of the SMT components.

1. Tin/silver/copper alloy (SAC305) with no clean chemistry flux (from two different suppliers)

2. Tin/silver/copper alloy (SAC305) with organic acid chemistry flux

3. Tin/lead alloy with no clean chemistry flux for baseline purposes

Three different solder alloys were used in this research for the assembly of the THT components. The solders to be used are as follows:

1. Tin/silver/copper alloy (SAC305)

2. Tin/copper alloy (Sn100C) using two different assembly operation settings. This solder has the same composition as the HASL alloy.

3. Tin/lead alloy for baseline purposes

Two different laminate materials were used for this research:

1. The first FR-4 laminate material was designed for use in lead-free assembly environments and has a glass transition (T_g) temperature of 180 degrees C. This laminate material was used for the 32 test vehicles included in the Design of Experiments.

2. Three test vehicles were assembled using laminate material with halogen-free flame retardants and a glass transition (T_g) temperature of 180 C.

Design of Experiments (DoE) is a systematic method for determining the effect of factors and their possible interactions on a design or process. [3] The three factors under investigation in the DoE were SMT solder paste, THT component solder, and surface finish. The four levels for the through THT solder factor were the SAC 305 tin/silver/copper alloy, Sn100C tin/copper alloy (at two different operational settings), and tin/lead alloy. The four levels for the SMT component solder paste were tin/silver/copper alloy (SAC305) with no clean flux (two different manufacturers used), tin/silver/copper alloy (SAC305) with organic acid flux, and tin/lead alloy with no clean flux. The four levels for the surface finish were ENIG, OSP, nano, and lead-free HASL. Table 3 shows the total of 24 lead-free experiments used in this research.

The DoE (including solder paste, solder, surface finish, and laminate material) that was used for the eight tin/lead test vehicles is provided in Table 4. These tin/lead test vehicles provided a baseline for comparison with the lead-free test vehicles.

Test	SMT Solder	Through	Surface	P\//R
Vehicle	Paste	Hole Solder	Finish	Laminate
1	SAC305 No Clean (1)	SAC305	ENIG	High Tg FR4
2	SAC305 No Clean (1)	SAC305	ENIG	High Tg FR4
3	SAC305 No Clean (1)	SAC305	LF HASL	High Tg FR4
4	SAC305 No Clean (1)	SAC305	LF HASL	High Tg FR4
5	SAC305 No Clean (1)	SAC305	OSP	High Tg FR4
6	SAC305 No Clean (1)	SAC305	OSP	High Tg FR4
7	SAC305 No Clean (1)	SAC305	Nano- finish	High Tg FR4
8	SAC305 No Clean (1)	SAC305	Nano- finish	High Tg FR4
9	SAC305 Org. Acid	Sn100C (295 C)	ENIG	High Tg FR4
10	SAC305 Org. Acid	Sn100C (295 C)	ENIG	High Tg FR4
11	SAC305 Org. Acid	Sn100C (295 C)	LF HASL	High Tg FR4
12	SAC305 Org. Acid	Sn100C (295 C)	LF HASL	High Tg FR4
13	SAC305 Org. Acid	Sn100C (295 C)	OSP	High Tg FR4
14	SAC305 Org. Acid	Sn100C (295 C)	OSP	High Tg FR4
15	SAC305 Org. Acid	Sn100C (295 C)	Nano- finish	High Tg FR4
16	SAC305 Org. Acid	Sn100C (295 C)	Nano- finish	High Tg FR4
17	SAC305 No Clean (2)	Sn100C (310 C)	ENIG	High Tg FR4
18	SAC305 No Clean (2)	Sn100C (310 C)	ENIG	High Tg FR4
19	SAC305 No Clean (2)	Sn100C (310 C)	LF HASL	High Tg FR4
20	SAC305 No Clean (2)	Sn100C (310 C)	LF HASL	High Tg FR4
21	SAC305 No Clean (2)	Sn100C (310 C)	OSP	High Tg FR4
22	SAC305 No Clean (2)	Sn100C (310 C)	OSP	High Tg FR4
23	SAC305 No Clean (2)	Sn100C (310 C)	Nano- finish	High Tg FR4
24	SAC305 No Clean (2)	Sn100C (310 C)	Nano- finish	High Tg FR4

Table 3: Lead-free Test Vehicles - Design of Experiments

Test Vehicle	SMT Solder Paste	Through Hole Solder	Surface Finish	PWB Laminate
25	Tin Lead No Clean	Tin/Lead	ENIG	High Tg FR4
26	Tin Lead No Clean	Tin/Lead	ENIG	High Tg FR4
27	Tin Lead No Clean	Tin/Lead	LF HASL	High Tg FR4
28	Tin Lead No Clean	Tin/Lead	LF HASL	High Tg FR4
29	Tin Lead No Clean	Tin/Lead	OSP	High Tg FR4
30	Tin Lead No Clean	Tin/Lead	OSP	High Tg FR4
31	Tin Lead No Clean	Tin/Lead	Nano- finish	High Tg FR4
32	Tin Lead No Clean	Tin/Lead	Nano- finish	High Tg FR4

.

In addition, three halogen-free test vehicles were assembled, but were not included within the DoE. The solder paste, solder, surface finish, and laminate materials that were used for the three halogenfree test vehicles are provided in Table 5.

SMT Solder Paste	Through Hole Solder	Surface Finish	PWB Laminate
SAC305 No Clean (1)	SAC305	OSP	Halogen- free FR4
SAC305 No Clean (1)	SAC305	OSP	Halogen- free FR4
SAC305 Org. Acid	SAC305	OSP	Halogen- free FR4
Table 5: Halogen-	froo Boards		

Table 5: Halogen-free Boards

Printing and Placement Process

The equipment used for printing operations was the DEK 265 printer using Instinctiv software. The bottom stencil used for this research was an electroformed nickel stencil with a thickness of 0.005", and the top stencil was an electroformed nickel stencil with a thickness of 0.004". The printing parameters used on the DEK 365 printer included a print speed of 0.51 inches per second, a front and rear blade pressure of 19.404 pounds, a separation speed of 0.055 inches per second, and a separation distance of 0.098 inches. These printing parameters were used for assembly of all the lead-free and tin/lead test vehicles. The GSM Genesis machine was used for placing the SMT components.

Reflow Process

The equipment used for reflow operations was the Vitronics Soltec XPM2 reflow oven with ten heating zones and three cooling zones, using Vitronics X2series XN1030 software. All profiles were done in an air environment which is less expensive and more prevalent in the industry than a nitrogen atmosphere. The thermal profile used for the tin/lead and lead-free test vehicles was a ramp to peak profile. Six thermocouples were attached to various locations of a spare test vehicle to develop the desired thermal profiles. Table 6 provides the component and test vehicle location information for the six thermocouple locations for the bottom side of the test vehicle.

Thermo- couple	Component Type	Reference Designator	Location on Test Vehicle
1	Resistor	RN12	Leading edge, center
2	Capacitor	С9	Center, right side
3	Resistor	RN9	Trailing edge, left side
4	Thin small outline package (TSOP)	U24	Center, left side
5	TO220	Q22	Trailing edge, center
6	Not applicable	Laminate	Center

Table 6: Test Vehicle Bottom Side Thermocouple Locations

There were six thermocouple locations used for developing the thermal profile for reflow of the top side of the test vehicle. Table 7 provides the component and board location information for these six thermocouple locations.

Thermo- couple	Component Type	Reference Designator	Location on Test Vehicle
1	Thin shrink small outline package (TSSOP)	U5	Trailing edge, right side
2	Capacitor	C3	Center
3	Resistor	RN5	Leading edge, center
4	Small outline	U23	Trailing edge, left side
5	Thin small outline package (TSOP)	U1	Trailing edge, center
6	Ball grid array (BGA)	U19	Center, left side

Tabla	7.	Toct	Vohiclo	Ton	Sido	Thormocounly	o Locations
Iable		ICSU	venicie	IUP	JIUC	mermocoupi	e Locations

The first temperature profile was developed for tin/lead test vehicles. The melting temperature for tin/lead solder is 183 °C. The target peak temperature in the reflow oven for test vehicles assembled with tin/lead solder is in the range of 210 to 218 °C, and the target time above liquidus (TAL) temperature is in the range of 60 to 90 seconds. The actual bottom side temperature profile for each of the six thermocouple locations can be seen in Figure 2.



Figure 2: Bottom Side Reflow Profile for Tin/Lead Boards

The second temperature profile generated was for the top side of the test vehicles assembled with tin/lead solder paste. The top side of the test vehicles contains BGA components that have lead-free solder balls. Therefore, a hybrid temperature profile was needed to melt the tin/lead solder pastes as well as the lead-free solder on the BGA components. The target peak temperature for the hybrid profile was in the range of 222 to 230 °C, and the target TAL was in the range of 60 to 90 seconds [4].

The third temperature profile generated was for the lead-free test vehicles. Lead-free solder paste using the SAC 305 tin/silver/copper alloy solder melts between 217 and 221 °C. All three lead-free solder pastes in this research contained the SAC 305 alloy. The target peak temperature for boards assembled with lead-free solder is in the range of 240 to 248 °C, and the target TAL is in the range of 60 to 90 seconds [5].

Assembly of Through Hole Components

The equipment used for this step was the Vitronics My Selective 6748 and 6749 soldering machines. This equipment has robotic multiwave and selectwave soldering capability and both methods were used for creating the solder joints for all the through hole components on the test vehicles. The selectwave process uses a robot system to pick up, hold, and drag the test vehicle over a single nozzle wave.

The multiwave process uses a robot system to pick up, hold, and dip the test vehicle onto multiple nozzles that are mounted on a product specific nozzle plate. The preheat temperature cannot be too high or it may burn off the flux before the soldering occurs. Therefore, the target preheat temperature used for this research was between 110 to 115 °C. A summary of the soldering parameters used for the thirty-two lead-free and tin/lead test vehicles in the DoE are provided in Table 8.

Parameter	SAC 305	Sn100C (1)	Sn100C (2)	Tin/Lead
Test Vehicle Number	1 - 8	9 - 16	17 - 24	25 - 32
Flux	Alpha 3215 NC	Alpha 3215 NC	Alpha 3215 NC	High Grade 1076-30 NC
Preheat	110– 115°C	110- 115°C	110- 115°C	110-115°C
Multiwave Pot Temp.	295°C	295°C	310°C	270°C
Multiwave Dwell Time	13 seconds	13 seconds	16 seconds	7 seconds
Selectwave Pot Temp.	300°C	300°C	310°C	270°C
Selectwave Nozzle Size	8 mm	8 mm	8 mm	4 mm

Table 8: Through Hole Soldering Parameters

The drag speeds used during the selectwave process were varied for the different component types and the different solder alloys. Table 9 provides the drag speeds used for the various component types and solders.

Compo- nents	SAC305 (mm/sec)	Sn100C(1) (mm/sec)	Sn100C(2) (mm/sec)	Tin/Lead (mm/sec)
Test Vehicle #	1 - 8	9 - 16	17 - 24	25 - 32
Capacitors	1.2	1.2	1.0	1.0
LEDs	1.2	1.2	1.0	1.0
TO220	2.0	2.0	1.7	5.0
DC/DC Converter	0.7	0.7	0.5	0.5

Table 9: Selectwave Drag Speeds

Inspection

The inspection effort included both visual and automated X-ray inspection. The IPC-A-610 Revision D standard was used as the guideline for conducting the visual inspection for this research. A defect is defined by this standard as a condition that may be insufficient to ensure the form, fit or function of the assembly in its end use environment. For this research, only soldering related defects were included. This includes the following defects: tombstoned, excess solder, insufficient solder, solder bridge, solder balls, non-wetting to pad, pinholes, unsoldered lead, icicles, cold solder, disturbed solder, solder splatter, and non-wetting to the component.

The visual inspection was conducted to meet the requirements of Class 3: High Performance Electronic Products. This classification was chosen because it covers electronics assemblies that must meet high reliability applications. The definition of Class 3: High Performance Electronic Products is as follows: "includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support and other critical systems" [6].

The visual inspection included the solder joints, the laminate, and components with the latter two being inspected for thermal degradation which is necessary because lead free processing temperatures are approximately 30°C higher as compared to assembly with tin/lead solder. The HP/Agilent 5DX X-ray system was used for the automated X-ray inspection. All assembly defects identified during the inspection process were at the component lead level. For example, if defects were found on three different leads of a single component, then the total defect count would be three.

RESULTS AND DISCUSSION

SMT Component Analysis

A total of 145 SMT component defects were identified on the thirty-five test vehicles resulting in an overall mean defect rate of 4.1 defects per test vehicle. The printed circuit boards, components, and flux residues (no-clean only) did not exhibit any signs of thermal degradation. Figure 3 shows an example of a surface mount component defect identified during this research. The resistor located at R1 on test vehicle is shown with a tombstone defect. R1 is the middle resistor in the picture.



Figure 3: Tombstone Defect on Test Vehicle 29

Minitab Software was used to generate all the statistical data and plots for this research. Upon review of the main effects plot for SMT components shown in Figure 4, it can be seen that the SAC 305 OA solder paste had a much higher mean defect rate (8.0 defects per board) than the overall average of 4.1 defects per board. The other three solder pastes had defect rates between 2.7 and 3.2 defects per board. For the surface finishes, it can be seen that the nano surface finish had the lowest mean defect rate (2.7 defects per board), while the other three surface finishes had defect rates between 4.0 and 5.5 defects per board.



Figure 4: Main Effects Plot for SMT Components

The interaction results for SMT components are shown in Figure 5. The combination with the lowest mean defect level was the tin/lead solder paste and the nano surface finish with zero defects per test vehicle. The combination with the highest defect level was the SAC 305 OA solder paste and the OSP finish with 10 defects per test vehicle.

This interaction plot shows that although the nano surface finish had the lowest overall defect rate, it had the highest defect rate for the SAC 305 NC2 solder paste. This plot also reveals that the Leadfree HASL surface finish had the lowest defect rate for both the SAC 305 NC1 and SAC 305 NC2 solder pastes. Based upon the results of this plot it can be stated that the Lead-free HASL was the best performing finish for lead-free no clean solder pastes, and that the nano finish was the best performing finish for the lead-free OA and tin/lead solder pastes.



Figure 5: Interaction Plot for Surface Mount Component Defects (All Solders)

Figure 6 is a Pareto Chart for the SMT component defect types for lead-free test vehicles only. This chart reveals that solder bridges, unsoldered leads, insufficient solder, and non-wetting to component were the most prevalent defect categories. The "Other Category" includes two voiding defects, one solder splatter defect, one non-wetting to pad defect, and one tombstoned defect.



Figure 6: Pareto Chart for SMT Component Defect Types for Lead-free Test Vehicles

Table 10 shows the relationship between the SMT component defect types for lead-free test vehicles and the four different surface finishes. For example, for the insufficient solder defect, the best performing surface finish was lead-free HASL with only one defect. For this defect type, the OSP surface finish had the highest number of defects with sixteen defects.

Surface Finish	Solder Bridge	Un- soldered Lead	Insufficient Solder	Non- wetting to Component
ENIG	11	11	5	3
LF HASL	7	5	1	6
OSP	7	4	16	7
Nano	5	9	3	0
Total	30	29	25	16
Total Table 10: C	30 Componer	29 nt Defect Typ	25 es by Surface F	16 inish

Figure 7 is a Pareto Chart for the surface mount component defect types for tin/lead test vehicles only. The chart reveals that solder bridges and tombstoning were the only defect categories found for tin/lead test vehicles.



Figure 7: Pareto Chart for SMT Component Defect Types for Tin/lead Test Vehicles

The three halogen-free test vehicles that were assembled had only one surface finish (OSP) and two different solder paste materials (SAC305 NC1 and SAC305 OA). Consequently, only four test vehicles (numbers 5, 6, 13, and 14) in the Design of Experiments with an OSP finish and either the SAC 305 NC1 or SAC305 OA solder pastes were used for the comparison with the halogen free boards. The mean defect level for the four selected High T_g FR4 laminate material (7.2 defects per board), was more than twice as high as the mean defect level for the halogen free laminate material (3.0 defects per board).

THT Component Analysis

Due to drift that occurred during the multiwave operations, only sixteen test vehicles were included in the THT DOE (only one replicate for each combination). A total of 1,685 THT component defects at the lead level were identified, and the overall mean for defects per board for all DoE combinations was 105.3 defects per test vehicle. Figure 8 shows an example of a THT component defect identified during this research and illustrates the insufficient solder defect for one of the leads of component Q17 on the topside of test vehicle number 22.



Figure 8: Insufficient Solder on Test Vehicle Number 22

The two best performing solders were Sn100C (1) and the SAC305 solders with 79.25 and 95.75 defects per test vehicle respectively. The two lesser performing solders were tin/lead and Sn100C (1) solders with 115.5 and 130.7 defects per test vehicle respectively. The two best performing surface finishes were lead-free HASL and ENIG surface finishes with 51.5 and 83.7 defects per test vehicle respectively. The two lesser performing surface finishes were the OSP and nano surface finishes with 142.5 and 143.5 defects per test vehicle respectively. The results of the main effects are shown in Figure 9.



Figure 9: Main Effects Plot for THT Component Defects

The interaction plot for the THT DoE reveals that the ENIG surface finish had the lowest defect rate when using the SAC305 and tin/lead solders. However, the ENIG surface finish had the highest defect rate when used with the Sn100C (1) and Sn100C (2) solders. The lead-free HASL had the lowest defect rate for the Sn100C (1) and Sn100C (2) solders. This positive result was expected given that the lead-free HASL finish is comprised of the Sn100 solder alloy. The performance of the nano and OSP surface finishes were comparable for each of the four solders. Figure 10 illustrates the effect of the THT DoE interactions for the various combinations.



Figure 10: Interactions Plot for THT Component Defects

For the tin/lead boards, 98.5% of the defects were either insufficient solder or solder bridging. For the assembly of THT components with lead-free solder, the most prevalent defect type was insufficient solder (53.6%), the second most prevalent was solder bridge (37%), and the third most was solder splatter (5.5%).

In addition, a comparison was made of the THT components in the three halogen-free test vehicles versus the corresponding two test vehicles (numbers 5 and 6) in the DoE that had similar factors. The mean defect level for the High T_g FR4 laminate material (177.5 defects per test vehicle), was 36% more than the mean defect level for the halogen free laminate material (130.3 defects per test vehicle).

TECHNOLOGY SPECIFIC CONCLUSIONS

SMT Solder Paste Conclusions

• For assembly of test vehicles using SMT components, no statistically significant difference was found for the 3 solders or within the 4 surface finishes used.

• Overall, the test vehicles assembled with the SAC 305 NC1 solder paste had the lowest defect rate for all the solder pastes evaluated in this research.

• For test vehicles assembled with lead-free solder pastes, the nano and lead-free HASL surface finishes had the lowest defect rate.

• For the various lead-free solder paste and surface finish combinations, the combination of SAC305 NC1 solder paste and the lead-free HASL surface finish had the overall lowest defect rate for the test vehicles assembled for this research.

THT Solder Conclusions:

• For the assembly of test vehicles using THT components, there was no statistically significant difference for the type of solder, but there was a statistically significant difference for the type of surface finish.

• The most prevalent defect categories identified for THT components were solder bridging and insufficient solder.

• Overall, the test vehicles assembled with the Sn100C-1 (first operating parameters) solder had the lowest defect rate for all three solders evaluated in this research.

• For test vehicles assembled with lead-free solders, Sn100C-1 solder had the lowest defect rate, and the HASL surface finish had the lowest defect rate.

• There was significant variation with the performance of the ENIG surface finish with the various solders. For the tin/lead and SAC305 solders, ENIG was the surface finish with the least defects, and for both Sn100C solder parameters, ENIG was the surface finish with the most defects.

Surface Finishes Conclusions:

• For THT component assembly, the test vehicles assembled with the OSP and nano surface finishes had the highest level of defects. For the test vehicles with an OSP finish, a contributor to this high failure rate was the time delay between conducting the SMT component assembly and THT component assembly. During this delay, there is potential for degradation of the OSP surface finish that can have a negative impact on subsequent soldering efforts. A key recommendation is to try to minimize the time delay between SMT and THT component assembly efforts. Preferably, both efforts should be conducted during the same day.

• The standard method for applying the nano surface finish to PCBs is to apply it directly to bare copper. However, for the test vehicles used in this research, this method was not followed due to unforeseen logistical issues. Instead, an OSP finish was first applied to the test vehicle, then the OSP finish was stripped off, and then the nano surface finish was applied to the test vehicles. The soldering results would most likely be better if the nano surface finish is applied directly to bare copper for further research or assembly efforts.

Overall Conclusions

• The defect rate was much higher for THT components than for SMT components. This indicates that further process optimization is needed for assembly of THT components using lead-free materials.

• The IPC-A-610D Class 3 standard for high reliability applications was used for inspecting the test vehicles assembled for this research. The assembly of lead-free electronics for high reliability applications is achievable with equal or less solder joint defects than tin/lead assemblies. This is viable with the careful selection of both lead-free solder and surface finish materials.

FUTURE WORK

Additional failure analysis will be performed on components, solder joints and laminates to determine the exact individual causes of reliability failures. The data will be investigated through statistical significance in order to expand the reliability analysis.

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BIOGRAPHIES



Dr. Gregory Morose has been managing the efforts of the New England Lead-free Electronics Consortium since 2004. Previously, Gregory had worked for several years in the electronics industry in various engineering positions. He has published and presented numerous papers about lead-free electronics research and implementation. He is also an ASQ certified Six Sigma Black Belt.



Dr. Sammy G. Shina, P.E., is a professor of Mechanical Engineering at the University of Massachusetts Lowell and the founder of the New England Lead Free Consortium. He is the author of four books on Concurrent Engineering, Six Sigma and Green Electronics Design and more than 100 papers on electronics assembly, quality, design, and manufacturing.



Robert Farrell is an Advanced Engineer who has been on the Benchmark Electronics Corporate Lead-free team since 2002 and has worked onsite at several Benchmark global locations as they converted from tin lead assembly to lead free. Bob has been an active member of the New England Lead Free Electronics Consortium since 2004. He has published and presented several lead

free technical papers and has a Masters of Science in Mechanical Engineering from Worcester Polytechnic Institute.

ELECTROLESS NI/PD/AU PLATING FOR PACKAGE SUBSTRATES WITH FINE PITCH WIRING

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ABSTRACT

Electrolytic Ni/Au films are typically used for solder ball and Au-wire bonding at the Cu terminals of semiconductor package substrates. We investigated the minimum Ni film thickness required for solder ball joint reliability after thermal aging. We verified the joint reliability using a high-speed solder ball shear test which is highly correlated with drop tests. We found that the minimum Ni-P thickness of electroless Ni-P/Pd/Au that can afford the required solder ball joint reliability is 1 μ m, whereas in the case of electrolytic Ni/Au, the minimum Ni thickness is 3 μ m. This result indicates that electroless Ni-P/Pd/Au plating is more suitable for highdensity wiring, as compared to electrolytic Ni/Au plating.

Furthermore, we investigated the cause of the poor ball-joint reliability of the case of electroless Ni-P/Pd/Au whose Ni-P thickness was thinner than 1 µm, comparing with that of bare Cu. In the case of the 0.1-µm-thick Ni-P, Cu-Sn intermetallic compounds (IMCs) of (Cu, Ni)₂Sn and (Cu, Ni)₆Sn₅ were formed after thermal aging. It was found that the average thicknesses of the Cu-Sn IMCs in the case of bare Cu and 0.1-µm-thick Ni-P were equal regardless of the thermal aging time. However, in the case of Cu-Sn IMCs containing microscopic amounts of Ni, the growth of (Cu, Ni)₂Sn was prevented but that of (Cu, Ni)₆Sn₅ was promoted. It was clear from focused ion beam / secondary ion microscopic (FIB/SIM) and electron back-scatter patterns (EBSP) observations that the grain sizes of (Cu, Ni)₂Sn and (Cu, Ni)₆Sn₅ were smaller than those of Cu₃Sn and Cu₆Sn₅, respectively. We consider that the small grain size of (Cu, Ni)₂Sn and (Cu, Ni)₂Sn₅ IMCs with a lot of grain boundaries might be the reason for the poor reliability of the solder ball joints. In the case of the 0.3-µm-thick Ni-P, the Ni-P film remained after the solder ball reflow process; however, voids formed and grew at the Cu/Ni-P interface with the thermal aging time. We suppose that the voids may be the cause of the poor adhesion at the interface.

Key words: Electroless Ni-P/Pd/Au, Solder joint reliability, Intermetallic compound (IMC), Thermal aging test, High-speed solder ball shear test

INTRODUCTION

Recently, there have been remarkable advances in the miniaturization, weight reduction, and multifunctionality of portable devices. To realize the advance, the area type surface mount of devices such as CSPs (Chip Size Packages) and BGAs becomes the main current in semiconductor packages.



Figure 1: Structure of the Electronics Package (Wire Bonding Type)

Fig. 1 shows the typical structure of an electronic package. The semiconductor chips are connected to the package substrate by gold wire bonding, and the package substrate is in turn connected to the printed circuit board by solder ball joints. In order to satisfy the required reliability for the connections, gold plating is applied to the terminal surfaces on both sides of the package substrate.

Conventional electrolytic Ni/Au plating is a mature technology, which has long been used for the surface finishing of package substrates. However, this technique cannot be suitably applied to high-density package substrates because it requires bus lines to every terminal and the necessary area for those lines. Therefore, electroless Ni-P/Au plating was adopted because it does not require bus lines. However, drop tests revealed that the ball joint reliability of the technique was insufficient. To solve the problem, we adopted electroless Ni-P/Pd/Au plating for the surface finishing of the terminals of the package substrates1-2).



Figure 2: Terminal for Wire Bonding

Figure 2 shows the high-density wiring with a terminal space of 20 μ m or less. In the case of high-density wiring such as that considered here, electroless Ni-P/Pd/Au plating of a conventional thickness of 3–5 μ m may cause short circuit failures.

In the previous papers, the detail of the influence of the Ni thickness on the solder joint reliability had not been clarified3-13). For this reason, we reported the influence of the Ni thickness and reflow cycles on the solder joint reliability14). In this report, we investigated the Ni thickness and thermal aging on the joint reliability to clearly identify the lower limit of electroless Ni-P thickness.

EXPERIMENTAL

Sample Preparation

A test pattern was formed on an epoxy resin copper clad laminate (MCL-E-679F; Hitachi Chemical Co., Ltd) using the semi-additive method. The thicknesses of the board and the copper foil were 0.6 mm and 3 µm, respectively. Then, a solder resist was formed to cover the circumference of the ball pad. The opening diameter of the ball pad was 0.63 mm. In the case of electroless Ni-P/Pd/Au plating, the thicknesses of each layer were as follows: Ni-P = 0.1, 0.3, 1, 2, 3, and 5 μ m; Pd = 0.1 μ m; and Au = 0.3 μ m. In the case of electrolytic Ni/Au plating, the thicknesses of each layer were as follows: Ni = 0.1, 0.3, 1, 2, 3, and 5 µm and Au = 0.3 µm. A bare copper substrate (without surface finishing plating) was also prepared. After applying flux, Pb-free solder balls (Sn3.0Ag0.5Cu, mass%) were attached to the test substrates and passed through a nitrogen reflow furnace (maximum temperature: 252°C). Ball shear tests were performed before and after thermal aging (100, 300, 500, and 1000 h at 150°C).

Reliability Test of Solder Ball Joints

As shown in Fig. 3, the distance between the shear tool tip and the package substrate was 50 µm. The shear speed was 200 mm/s. A DAGE 4000HS Bondtester (Dage Precision Industries, Ltd.) was used (Fig. 4). The fracture surface was observed with an optical microscope and the modes were classified into ductile and brittle, as shown in Fig. 5. Typical shear force-displacement curves of these modes are shown in Fig. 6. There is a small difference in the peak force but a large difference in the shear energy, which was calculated from the integration of these curves. The ratio of the ductile fracture modes to the total number of fracture was defined as the ductile fracture ratio DFR (%).



Figure 3: Outline of Solder-Ball Shear Test



Figure 4: Externals of High-speed Shear Test Equipment (DAGE 4000HS Bond Tester)



Figure 5: Classification of the Fracture Mode for Solder Ball Shear Test (a) Ductile Fracture Mode, (b) Brittle Fracture Mode



Figure 6: Typical shear force-displacement curve of ductile and brittle fracture modes

RESULTS AND DISCUSSION

Influence of Ni Thickness on Reliability of Solder ball Joints

The influence of the Ni thickness on the reliability of solder ball joints was investigated. Fig. 7 shows the DFR obtained with the electrolytic Ni/Au and electroless Ni/Pd/Au varing thermal aging time. In the case of an electrolytic Ni film with a thickness of 0.1-1µm, the DFR decreased with an increase in the thermal aging time. In the case of the 2-µm-thick electrolytic Ni film, the fracture mode was ductile within 100 h of thermal aging but brittle after 1000 h of aging. The joint reliability for a thickness of 3 µm or more was equal to that for an actual thickness of 5 µm.



Figure 7:The Dependence of the Failure Mode on Ni Plating and Thermal Aging.

Thermal Aging Times: a = 0 h, b = 100 h, c = 300 h, d = 500 h, e = 1000 h

Fracture Mode: Ductile (light shading) Brittle (dark shading)



Figure 8: Cross-sectional FE-SEM Images of IMC after Various Thermal Aging Time at 150°C. Thickness of Ni or Ni-P: 1µm.

In the case of 0.1-µm-thick and 0.3-µm-thick electroless Ni-P layers, the failure mode was brittle after 300 h of aging. The level of reliability of the solder ball joint with a 1-µm-thick electroless Ni film was similar to that obtained for an electrolytic Ni film with a thickness of 3-µm or more. Consequently, the minimum electroless Ni-P thickness for a reliable solder ball joint was found to be 1 µm. In the case of a bare Cu terminal surface, the DFR decreased with an increase in the thermal aging time. It was found that the joint reliability for an electroless Ni-P film with a thickness of 1 µm or more and for an electrolytic Ni film with a thickness of 3 µm or more was slightly higher than that for bare Cu. Fig. 8 shows the result of the FE-SEM observations with different aging times. In the case of electrolytic Ni, the Ni film was partially diffused after 500 h, and almost the entire Ni film diffused; further, a thick intermetallic compound (IMC) (Sn/Cu/Ni = 51/44/5 mass%) was formed after 1000 h. In contrast, in the case of electroless Ni-P, the Ni-P film remained intact after 1000 h. Thus, an electroless Ni-P film can be considered as an excellent barrier film on a Cu layer, as compared to an electrolytic Ni film. Moreover, we had previously reported that a 2-µm-thick uniform electroless Ni-P plating was applicable to 10µm-spaced Cu wiring without a stray plate14). Therefore, electroless Ni-P/Pd/Au plating is suitable for high-density wiring.

Failure Analysis

In electroless Ni-P/Pd/Au plating with Ni thickness less than 1 μ m, DFR decreased significantly; the value was less than that of bare Cu. The following examinations were carried out for the further study.

Figure 9	Peak strength(N)	Shear energy(mJ)
(a)	26.0	21.9
(b)	24.5	8.3
(c)	20.1	2.6
(d)	8.1	0.5

Table 1: Ball shear peak strength and energy of different failure modes at Figure 9



Figure 9 Ball shear force-displacement curve for different Ni-P film thickness, after thermal aging at 150°C Thermal aging time: 1000 h

- (a) Bare Cu with ductile fracture mode
- (b) Bare Cu with brittle fracture mode
- (c) 0.1 µm thick Ni-P with brittle fracture mode
- (d) 0.3 µm thick Ni-P with brittle fracture mode



Figure 10: Brittle Fracture Surface after High-Speed Solder Ball Shear Test. Shear speed: 200 mm/s, Aging time: 1000 h(150°C) (b) Bare Cu, (c) Ni-P 0.1 μ m

(1) Solder ball shear force and shear energy

Fig. 9 shows typical ball shear force-displacement curves after 1000 h of aging. Table 1 summarizes the ball shear peak force and shear energy obtained from Fig. 9.

For a 0.1-µm-thick Ni-P film (c), the shear energy was about one-third of that of bare Cu with brittle fracture (b).

For a 0.3-µm-thick Ni-P film (d), both the shear force and the shear energy were extremely low as compared to the values in other cases. In addition, bare Cu with ductile fracture had the largest shear force and shear energy.



Figure 11: Cross-Sectional FE-SEM Images of IMC after Various Thermal Aging Time at 150°C



Figure 12: Cross-Sectional EDX Element Mappings of IMC after Various Thermal Aging Time at 150°C

(2) Failure analysis for 0.1-µm-thick electroless Ni-P

Fig. 10 shows the FE-SEM images of the brittle fracture surfaces on the Cu pad in the cases of (b) and (c) of Fig. 9. In the case of bare Cu (Fig. 10 b), the surface roughness was greater than that in the case of 0.1-µm-thick Ni-P with the brittle fracture mode (Fig. 10 c). In the case of sample (b), two kinds of IMCs (Cu₃Sn and Cu₆Sn₅) were detected by energy dispersive X-ray (EDX) analysis.

In addition, a small amount of Ni (about 1 mass% or less) was detected in the two kinds of IMCs on the surface of (c). Therefore, these IMCs were considered to be $(Cu, Ni)_3Sn$ and $(Cu, Ni)_6Sn_5$ by composition. In addition, a small crystal size $(Cu, Ni)_6Sn_5$ particle was present in the flat surface of $(Cu, Ni)_3Sn$ in sample (c).

In order to investigate the growth of Cu-Sn IMCs, we observed a cross section of the interface of the solder and the Cu pad. Figs. 11 and 12 show cross-sectional FE-SEM images and EDX element mapping, respectively, of IMCs with different thermal aging times.

In the case of bare Cu, Cu₃Sn and Cu₆Sn₅ layers were formed with approximately equal thicknesses on the Cu pad. In contrast, in the case of 0.1- μ m-thick Ni-P, the Ni-P film was completely diffused during the solder ball reflow process, and thin (Cu, Ni)₃Sn and thick (Cu, Ni)₆Sn₅ layers were formed after 1000 h of aging.



Figure 13: Thickness of IMCs after Various Thermal Aging Time at 150°C (a) Bare Cu, (b) Ni-P 0.1 µm

We measured the thickness of two kinds of Cu-Sn IMCs using FIB/SIM images. The results are shown in Fig. 13. In the case of bare Cu (Fig. 13 a), the overall thickness of the Cu-Sn IMCs increased to 8.4 µm from an initial thickness of 2.0 µm, after 1000 h of aging. The Cu₆Sn₅ layer was thicker than the Cu₃Sn layer till an aging time of 300 h, while the thicknesses of the Cu₂Sn₅ and Cu₂Sn layers were almost similar after 500 h of aging. In the case of 0.1-µm-thick electroless Ni-P (Fig. 13 b), Cu-Sn IMCs thickened to 8.2 µm from an initial thickness of 2.0 µm after 1000 h of aging. As compared to the Cu₃Sn layer, the (Cu, Ni)₃Sn layer thickened to less than 2 µm after 1000 h of aging. It was found that the overall thicknesses of the Cu-Sn IMCs for bare Cu and 0.1-µm Ni-P were approximately equal regardless of the thermal aging time. However, for Cu-Sn IMCs that contained microscopic amounts of Ni, (Cu, Ni)₃Sn growth was prevented but (Cu, Ni)₆Sn₅ growth was promoted.

As seen in Fig.10, the IMCs grain sizes appear different. We verified the grain sizes by FIB/SIM and EBSP, whose results are shown in Figs. 14 and 15, respectively. It was clear that the grain sizes of $(Cu, Ni)_3$ Sn and $(Cu, Ni)_6$ Sn₅ were smaller than those of Cu₃Sn and Cu₆Sn₅. We suppose that the microscopic amount of Ni contained in the Cu-Sn IMCs prevented the crystal growth of Cu₂Sn and Cu₆Sn₅.

The hardness and the Young's modulus of the Cu-Sn IMCs were investigated by nanoindentation testing. The results are shown in table 2. The hardness of Cu-Sn IMCs was 20 or more times that of the solder, while its Young's modulus was two or more times that of the solder. The data show that the physical properties of Cu_3Sn and $(Cu, Ni)_3Sn$ are slightly higher than those of Cu_6Sn_5 and $(Cu, Ni)_6Sn_5$. Therefore, we infer that the microscopic physical property of Cu-Sn IMCs does not affect the solder joint reliability.



Figure 14: Cross-Sectional FIB/SIM Images of Cu3Sn and (Cu, Ni)3Sn after Thermal Aging at 150°C for 1000 h (a) Bare Cu, (b) Ni-P 0.1 μ m



Figure 15: EBSP Images of Cu6Sn5 and (Cu, Ni)6Sn5 after Thermal Aging at 150°C for 1000 h. (a) Bare Cu, (b) Ni-P 0.1 μ m

On the basis of the above results, we assumed the following fracture mechanism. The cross-sectional structure images of the Cu-Sn IMCs and destruction points images according to the shear test are shown in Fig. 16. Crystal growth by thermal aging was prevented for Cu-Sn IMCs containing microscopic amounts of Ni, and the grain sizes of $(Cu, Ni)_3Sn$ and $(Cu, Ni)_6Sn_5$ were smaller than those of Cu₃Sn and Cu₆Sn₅, respectively. The fracture point under drop condition was either at the grain boundary or inside the IMCs. We considered that brittle fracture may easily occur when many grain boundaries exist, even if the thickness of the IMC was the same. Therefore, the small grain size of (Cu, Ni)₃Sn and (Cu, Ni)₆Sn₅ may be the reason for the poor reliability of the solder ball joint.

IMC	Hardness(GPa)	Yang's Modulus(GPa)
Cu₃Sn	8.7	182
Cu₅Sn₅	7.5	140
(Cu,Ni)₃Sn	9.4	182
(Cu,Ni)₅Sn₅	7.2	136
Solder	0.28	58

Table 2: Hardness and Yang's Modulus of the IMCs



Figure 16: Cross Sectional Structure Images of the IMC and Destruction Points Images According to the Shear Test Aging time: 1000 h(150°C) (a) Bare Cu, (b) Ni-P 0.1 µm



Figure 17: Cross-Sectional FE-SEM Images of IMC after Various Thermal Aging Time at 150°C Ni-P: 0.3 µm

Aging time: (a) 0 h, (b) 300 h, (c) 500 h, (d) 1000 h



Figure 18: Cross-Sectional FIB/SIM Images of Solder Ball Joint Interface after Various Thermal Aging Time at 150°C Ni-P: 0.3 μm

Aging time: (a) 0 h, (b) 300 h



Figure 19: FE-SEM and EDX Element Mappings of Brittle Fracture Surfaces after Various Thermal Aging Time at 150°C Ni-P: 0.3 µm



Figure 20: Voids Generation Image with Increase in Aging Time at 0.3 μm thick Electroless Ni-P

(3) Failure analysis for 0.3-µm-thick electroless Ni-P

Cross-sectional FE-SEM images of IMCs after different thermal aging times with 0.3- μ m-thick Ni-P are shown in Fig. 17. Voids were partially formed after 300 h of aging, and continuous voids were formed after 500 h of aging. A thick IMC layer of (Cu, Ni)₆Sn₅ was formed after 1000 h of aging. We verified the presence of voids with the help of FIB/SIM images. Fig. 18 shows the solder ball joint interface after 300 h of aging. The voids formed after thermal aging are clearly observed, and the size is more significant after several reflow cycles, as previously reported³).

Additionally, Fig. 19 shows FE-SEM and EDX images of the brittle fracture surfaces. Only Cu existed at the brittle fracture surface after 300 h of aging. We assumed that voids were generated and grown by Cu diffusion from the Cu pad through the thin Ni-P boundary, as illustrated in Fig. 20. We conclude that the above mentioned void growth is the cause of the poor adhesion at the Cu/Ni-P interface.

CONCLUSION

The influence of Ni thickness on solder ball joint reliability after thermal aging was investigated in the cases of electrolytic Ni/Au and electroless Ni-P/Pd/Au films. The cause of the poor ball joint reliability for an Ni-P layer with a thickness of less than 1 µm was thoroughly examined, comparing with that of bare Cu. The following results were obtained:

(1) The level of the reliability of the solder ball joint with the 1 μ m thick electroless Ni-P film was the same as that of the 3 μ m or more thick electrolytic Ni film.

(2) In the case of 0.1- μ m-thick Ni-P, two kinds of IMC layers— (Cu, Ni)₃Sn and (Cu, Ni)₆Sn₅—were formed after thermal aging. The grain sizes of the IMC layers were smaller than those of bare Cu. The poor ball joint reliability appears to have been caused by the many grain boundaries in the IMCs.

(3) In the case of 0.3-µm-thick Ni-P, the solder ball joint reliability after thermal aging was extremely poor. The poor reliability may be due to the poor adhesion at the Cu/Ni-P interface caused by the creation of voids by Cu diffusion to the IMC passing through the boundaries of Ni-P.

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ACHIEVING HIGH RELIABILITY LOW COST LEAD-FREE SAC SOLDER JOINTS VIA MN OR CE DOPING

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ABSTRACT

In this study, the reliabilities of low Ag SAC alloys doped with Mn or Ce (SACM or SACC) were evaluated under JEDEC drop, dynamic bending, thermal cycling, and cyclic bending test conditions against eutectic SnPb, SAC105, and SAC305 alloys. The Mn or Ce doped low cost SAC105 alloys achieved a higher drop test and dynamic bending test reliability than SAC105 and SAC305, and exceeded SnPb for some test conditions. More significantly, being a slightly doped SAC105, both SACM and SACC matched SAC305 in thermal cycling performance. In other words, the low cost SACM and SACC achieved a better drop test performance than the low Ag SAC alloys plus the desired thermal cycling reliability of high Ag SAC alloys. The mechanism for high drop performance and high thermal cycling reliability can be attributed to a stabilized microstructure, with uniform distribution of fine IMC paricles, presumably through the inclusion of Mn or Ce in the IMC. The cyclic bending results showed SAC305 being the best, and all lead-free alloys are equal or superior to SnPb. The reliability test results also showed that NiAu is a preferred surface finish for BGA packages over OSP.

Keywords: Lead-free, solder, SnAgCu, SAC, Mn, Ce, reliability, drop, thermal cycling, bending

INTRODUCTION

Lead-free soldering has been widely adopted by the electronics industry, with SnAgCu (SAC) having high Ag content being the initial main stream of choice. This selection was challenged later by the fragility of solder joint toward drop and the high cost of Ag. Low Ag SAC was considered a solution for resolving both issues. However, this approach compromised temperature cycling performance, therefore is not acceptable for high end applications. In this study, low Ag SAC alloys doped with Mn or Ce were evaluated against eutectic SnPb, SAC105, and SAC305 for JEDEC drop, dynamic bending test, -40/125°C temperature cycling, and 1Hz/2mm cyclic bending tests. Prior to the drop and bending tests, a part of the samples were preconditioned with 150°C thermal aging or 250 cycles temperature cycling. The primary test vehicle employed was TFBGA with NiAu finish mounted on PCB with OSP finish.

EXPERIMENT

1. Assembly

(1) Solder Alloys:

Five solder sphere alloys were evaluated, including two new alloys, 98.5Sn1Ag0.5Cu0.05Mn (SACM) and 98.5Sn1Ag0.5Cu0.02Ce (SACC), and three controls, 63Sn37Pb (SnPb), 98.5Sn1Ag0.5Cu (SAC105), and 96.5Sn3Ag0.5Cu (SAC305).

For JEDEC drop test, thermal cycling test, and cyclic bending test, two no-clean solder pastes were used, SnPb and SAC305. The former was used for SnPb TFBGA mounting, while the latter was for lead-free TFBGA mounting.

For dynamic bending test, 95.5Sn3.8Ag0.7Cu (SAC387) noclean solder paste was used.

(2) Device Assembly:

For JEDEC drop test, temperature cycling test, and cyclic bending test, the following parts and reflow profiles were used.

Components: Daisy TFBGA244, 12X12, 0.3 mm ball/0.5 mm pitch, electrolytic NiAu (5 μ Ni and 0.2-0.5 μ Au), and OSP (0.2-0.4 μ). Unless otherwise specified, all work was done on NiAu.

PCB: High Tg FR4/8 layers/Non-Via In Pad (NVID)/Non-Solder Mask-Defined Pad (NSMD), with surface finishes of organic solderability preservative (OSP, 0.2-0.4 μ), electroless nickel immersion gold (ENIG, with 5 μ Ni and 0.1 μ Au), and Immersion silver (ImAg, 0.2 μ). Unless otherwise specified, all work was done on OSP.

Reflow profile for SnPb assembly: peak temperature 220°C, reflow under air.

Reflow profile for lead-free assembly: peak temperature 245°C, reflow under air.

For dynamic bending test, the following parts and reflow profile were used.

Components: Live TFBGA244, 12X12, 0.3 mm ball/0.5 mm pitch, electrolytic NiAu (5 μ Ni and 0.2-0.5 μ Au)

PCB: FR4/8 layer/NVIP/Solder Mask-Defined Pad (SMD), with OSP finish (0.2-0.4 $\mu).$

Reflow profile: ramp-to-peak, peak temperature 235°C, reflow under air.

2. Tests

Four tests were conducted in the evaluation of the solder materials.

(1) JEDEC Drop Test (JDT)

Fifteen packages were mounted on a 132 x 77 x 1 mm3 standard 8-layer JEDEC drop test board in a layout regulated by JEDEC, in which the mounted packages were individually numbered. The test board and each of the mounted packages were daisy-chain designed so that the overall electrical resistance of daisy-chained solder joints could be individually measured for each mounted package.

On the test PC board side, the solder joint was in a NSMD structural configuration. The diameter of the OSP coated Cu pad was 0.28 mm whereas the solder mask opening was 0.43 mm, following the requirement of JESD22-B111 for the pitch of solder joints at 0.5 mm.

The drop times were recorded for failed unit when resistance exceeding 1000 ohms.

As schematically shown in Fig. 1, the board-level test vehicle was affixed to the drop table at the four corners with the mounted packages facing downward, according to the regulation by JESD22-B111. The drop table was then released and dropped freely at a certain height to impact on the strike surface repetitively, each time creating a half-sine impact acceleration pulse of a peak acceleration of G0 (1500Gs) and duration of τ .(0.5 ms). Before each test the tightness of the test board should be checked to avoid experimental uncertainties as a result of extra vibrations of the board.

(2) Thermal Cycling Test (TCT)

The samples were subject to TCT (-40-125°C, 42 min/cycle, ramp up/down: 11 min, dwell time 10 min) with real time resistance monitoring. A failure was defined when a 20% resistance increase was recorded.



Figure 1: Schematic for JEDEC board-level drop test.



Figure 2: Board level cyclic bend test vehicle

Figure 3: Schematic showing 4-Point bending set-up & machine

(3) Cyclic Bending Test (CBT)

Nine packages were mounted on a 132x77x1 mm3 standard 8layer PC board with layout regulated by JESD22B113, as shown in the figure where the mounted package were numbered individually. The test board and mounted package was daisy-chain designed so that the overall electrical resistance of daisy-chain solders joints can be individually measured in each mounted package. Each cell was subject to cyclic bend test at 1 Hz/2mm testing condition until all components failure and the cycles number were recorded for failed unit when resistance exceeding 1000 ohms.

(4) Dynamic Bending Test (DBT)

A high strain rate drop test reported by Motorola [1-3] was adopted in this work to measure failure behavior of the second-level package reliability for mobile applications. This test was found to regenerate the failure mode of solder joints in surface mount devices found in the phone drop [4].

The test apparatus was composed of the 4-point bending setup. During testing the bending direction by connecting two opposite corner balls of the device was alignetd along the longitudinal direction of the PCB. The rollers of the bottom span of the 4point bending fixture were positioned 60 mm apart while the top span distance was 35 mm. A steel ball was dropped from various heights onto the top span fixture to induce various levels of strains in order to control stress levels at solder joints. The strain gauge was mounted on the back of the PCB, as shown in Fig. 4.



Figure 4: High strain rate 4 point dynamic bending setup.

The board strain was increased incrementally, and each unit was impacted only once. After the dynamic bending test, joint failure was identified by dye and pry process. The number of joint failures for each unit was collected for the given board strains, and the data set was fit to a Weibull curve to obtain the board strain level required to generate one solder joint failure.

Prior to the above tests, the devices were preconditioned with thermal aging at 150°C. Further more, drop test or cyclic bending test after TCT pretreatment was conducted. The DOEs for primary work are shown in Table 1 and Table 2.

Package			Daisy TFBG	A244 12X12					
Ball/pitch (mm)	0.3/0.5	0.3/0.5	0.3/0.5	0.3/0.5	0.3/0.5	0.3/0.5			
Solder ball	SnPb	SAC105	SAC305	SACM	SACM	SACC			
Surface finish of substrate	NiAu	NiAu	NiAu	NiAu	Cu/OSP	NiAu			
Solder paste	SnPb	SAC305	SAC305	SAC305	SAC305	SAC305			
Reflow profile	220C	245C	245C	245C	245C	245C			
PCB	High Tg FR4/8 layer/NVIP/NSMD/OSP								
Thermal aging 150C/0hr	TCT (.40/125) solder joint reliability								
	Drop solder joint reliability								
	Cyclic Bending (1Hz/2mm) solder joint reliability								
	TCT (-40/125) solder joint reliability								
Thermal aging 150C/100hr	Drop solder joint reliability								
	Cyclic Bending (1Hz/2mm) solder joint reliability								
	TCT (-40/125) solder joint reliability								
Thermal aging 150C/250hr	Drop solder joint reliability								
	Cyclic Bending (1Hz/2mm) solder joint reliability								
TOT (40/105/0 0501-	Drop solder joint reliability								
1C1 (-40/125C) 250 cycle	Cyclic Bending solder joint reliability								
Thermal aging(0/100/250hrs/1000hrs)	X-section vie	w for interfaci	ial IMC micro	structure in pa	ackage and PC	CB (OSP) side			

Table 1: DOE for JEDEC tests.

Package	e	Live TFBGA					
Ball/pitch (mm)	0.3/0.5	0.3/0.5	0.3/0.5	0.3/0.5		
Surface finish (s	NiAu	NiAu	NiAu				
Solder ba	SAC105	SAC305	SACM	SACC			
Solder pas	SAC387						
Reflow pro	Mountain profile (235C peak)						
PCB	FR4/8 layer/NVIP/SMD						
Thermal aging 150C/0hr	Dynamic bending	Dye and pry					
Thermal aging 150C/250hr	Dynamic bending	Dye and pry					

Table 2: DOE for 4 point dynamic bending test.

RESULTS

1. JEDEC Drop Test (JDT)

For devices with TFBGA (NiAu) assembled on PCB (OSP) pretreated with 250 cycles of TCT, the JDT performance of various sphere alloys is represented in Weibull plot shown in Fig. 5. The reliability can be ranked in the following order:

 $SACM \ge SnPb \ge SACC > SAC105 > SAC305$



Fig. 5 Weibull plot for JDT performance for TFBGA (NiAu) with various sphere alloys assembled on PCB (OSP). The device was pretreated with 250 cycles of TCT prior to JDT.

Fig. 6 and Fig. 7 show the characteristic life (C-Life) and first failure of JDT for TFBGA (NiAu) on PCB (OSP), respectively. Overall, the C-Life of alloys for as reflowed devices is ranked as:

SACC > SACM > SAC105 > SnPb > SAC305



Fig. 6 C-Life in JDT for TFBGA (NiAu) on PCB (OSP) cycled, the ranking of first failure is shown below.



Tigare 7. Thist familie in 301 for the box (NIAU) on FCB (USP)

On the other hand, the ranking of alloys on first failure for as reflowed devices is shown below.

SACC > SACM > SnPb > SAC105 > SAC305

For devices which have been thermally aged or temperature

SnPb > SACM > SACC > SAC105 > SAC305

Fig. 8 and Fig. 9 show the effect of package surface finish on the C-Life and first failure of JDT for TFBGA on PCB (OSP), respectively using SACM. Overall, for devices pretreated with 250 TCT, the JDT reliability of NiAu is better than OSP. However, for as reflowed devices or thermally aged devices, the JDT reliability of OSP is better than NiAu.



Figure 8: C-Life in JDT for TFBGA on PCB (OSP) for SACM.



Figure 9: First failure in JDT for TFBGA on PCB (OSP) for SACM

The effect of PCB surface finishes on JDT was studied for SACM and SACC. Fig. 10 shows the C-Life while Fig. 11 shows the first failure. In most cases, for as reflowed devices, the reliability of JDT shows the following order: ImAg > OSP > ENIG. For thermally aged or thermal cycled devices, the trend slightly changed: OSP > ImAg > ENIG in most instances.



Figure 10: Effect of PCB surface finish on C-Life of JDT for SACM and SACC for devices assembled with TFBGA (NiAu).



Figure 11: Effect of PCB surface finish on first failure of JDT for SACM and SACC for devices assembled with TFBGA (NiAu).

2. Thermal Cycle Test (TCT)

For devices with TFBGA (NiAu) assembled on PCB (OSP) and aged at 150C for 250 hrs, the TCT performance of various sphere alloys is represented in Weibull plot shown in Fig. 12. The reliability can be ranked in the following order:

 $SACC > SACM \ge SAC305 > SAC105 > SnPb$



Figure 12: Weibull plot for TCT performance for TFBGA (NiAu) with various sphere alloys assembled on PCB (OSP). Prior to TCT, the device was aged at 150C for 250 hrs.

Fig. 13 and Fig. 14 show the C-Life and first failure of TCT for TFBGA (NiAu) on PCB (OSP), respectively. Overall, the C-Life of alloys for as reflowed devices can be ranked below.

SAC305 > SACC, SACM > SAC105 > SnPb

However, for devices which have been thermally aged or thermal cycled, the ranking of C-life is shown below.

SACC ≥ SACM, SAC305 > SAC105 > SnPb

On the other hand, the ranking of alloys on first failure for as reflowed devices is shown below.

SnPb > SACC > SACM > SAC105 > SAC305

For devices which have been thermally aged or thermal cycled, the ranking of first failure is shown below.









Figure 14: First failure of TCT for TFBGA (NiAu) on PCB (OSP).

For SACM, the effect of package surface finish type on TCT reliability is shown in Fig. 15 and Fig. 16 for C-Life and first failure, respectively. NiAu is distinctly better than OSP in this case.



Figure 15: Effect of TFBGA surface finish on C-Life of TCT for BGA on PCB (OSP) for SACM.



Figure 16: Effect of TFBGA surface finish on first failure of TCT for BGA on PCB (OSP) for SACM.

The effect of PCB surface finishes on TCT was studied for SACM and SACC. Fig. 17 shows the C-Life while Fig. 18 shows the first failure. ENIG appears to be more noticeably poorer than the other two finishes. Overall, there is a weak trend showing ImAg > OSP > ENIG.



Figure 17: Effect of PCB surface finish on C-Life of TCT for SACM and SACC for devices assembled with TFBGA (NiAu).



Figure 18: Effect of PCB surface finish on first failure of TCT for SACM and SACC for devices assembled with TFBGA (NiAu).

3. Cyclic Bending Test (CBT)

For devices with TFBGA (NiAu) assembled on PCB (OSP) and aged at 150°C for 250 hrs, the CBT performance of various sphere alloys is represented in Weibull plot shown in Fig. 19. The reliability can be ranked in the following order:

SAC305 > SACC, SACM, SAC105 > SnPb



Figure 19: Weibull plot for CBT performance for as reflowed TFBGA (NiAu) using various sphere alloys assembled on PCB (OSP).

Fig. 20 and Fig. 21 show the characteristic life (C-Life) and first failure of CBT for TFBGA (NiAu) on PCB (OSP), respectively. Overall, the C-Life of alloys for as reflowed devices can be ranked below.

SAC305 >> SACM ≥ SACC, SAC105 > SnPb







However, for devices which have been thermally aged or temperature cycled, the ranking of C-life is shown below.

 $SAC305 > SAC105 \ge SACM$, $SnPb \ge SACC$

On the other hand, the ranking of alloys on first failure for as reflowed devices is shown below.

 $SAC305 > SACM > SAC105 \ge SACC > SnPb$

For devices which have been thermally aged or temperature cycled, the ranking of first failure is shown below.

SAC305 > SAC105 > SACM, SnPb > SACC

For SACM, the effect of package surface finish type on CBT reliability is shown in Fig. 22 and Fig. 23 for C-Life and first failure, respectively. For as reflowed or thermal cycled devices, NiAu is better than OSP. The trend vanishes for thermally aged devices.



Figure 22: Effect of TFBGA surface finish on C-Life of CBT for BGA on PCB (OSP) for SACM.



Figure 23: Effect of TFBGA surface finish on first failure of CBT for BGA on PCB (OSP) for SACM.

The effect of PCB surface finishes on CBT was studied for SACM and SACC. Fig. 24 shows the C-Life while Fig. 25 shows the first failure.



Figure 24: Effect of PCB surface finish on C-Life of CBT for SACM and SACC for devices assembled with TFBGA (NiAu).



Figure 25: Effect of PCB surface finish on first failure of CBT for SACM and SACC for devices assembled with TFBGA (NiAu).

For C-Life, a trend can be recognized: ImAg > OSP > ENIG. For first failure, ENIG appears to be more noticeably poorer than the other two finishes.

The Weibull data, β , η , and ρ , for JDT, TCT, and CBT for most of the systems are listed in Appendix 1.

4. Dynamic Bending Test (DBT)

For devices with TFBGA (NiAu) assembled on PCB (OSP), the DBT performance of various sphere alloys is shown in Fig. 26. The reliability for as reflowed devices can be ranked in the following order:

SACM > SACC > SAC105 > SAC305

However, for thermally aged (150°C/250 hrs) devices, the performance gap between doped SAC105 systems and regular SAC105 increases, and the ranking of alloys altered, as shown below.

SACM > SACC > SAC305 > SAC105



Figure 26: DBT performance for TFBGA (NiAu) on PCB (OSP).

5. Microstructure

Fig. 27 shows the microstructure of interface of solder joints of TFBGA (NiAu) on PCB (OSP) aged at 150°C. SACM and SACC displayed a thinner and smoother interfacial IMC layer than SAC105 at both package side and PCB side. SAC105 also exhibited a bulk solder dispersed with more coarse IMC particles than SACM and SACC.

Fig. 28 shows IMC thickness of BGA joints at packaging side (average of 3 balls) mounted on PCB (OSP). Among all, SACM on NiAu had the lowest IMC thickness. On the other hand, OSP showed a faster IMC growth rate than NiAu. This is consistent with other findings [5,6]. It is interesting to note that SACC on NiAu showed a thinner IMC but a similar growth rate as SACM on OSP.



Figure 27: Interface of solder joints of TFBGA (NiAu) on PCB (OSP) aged at 150°C.



Figure 28: IMC thickness of TFBGA joints at packaging side mounted on PCB (OSP).

The IMC thickness at PCB (OSP) side is shown in Fig. 29. Again, SACM exhibited the lowest IMC thickness among all, if the packaging side was NiAu. SACC showed a lower thickness than the rest systems, although the IMC growth rate was comparable.



Figure 29: IMC thickness of TFBGA solder joints at PCB (OSP) side.

The interfacial IMC morphology is shown in Fig. 30 for solder/ TFBGA (NiAu) interface for solder bumps aged at 150°C for various period of time. The solder has been selectively removed by etching, and the IMC at interface is exposed. For SAC105 and SAC305, the IMC rods grew thicker and longer considerably upon aging. SACM had slightly finer IMC particles than SAC alloys in the as reflowed joints. Those IMC particles thickened slower than both SAC alloys upon thermal aging. SACC showed similar behavior as SACM.

Fig. 31 shows the effect of alloy type and thermal aging pretreatment prior to TCT on the microstructure of thermal cycled devices. The optical micrographs indicate the IMC particles of SAC105 coarsened significantly by 150°C/250 hrs thermal aging prior to TCT. The IMC particle size and distribution of SACC without thermal aging are similar to SAC105. For SACM samples without thermal aging pretreatment, the IMC particles are much finer than SAC105, as can be seen in the close up look pictures in Fig. 32. Both SACC and SACM showed no coarsening of the IMC particles with thermal aging pretreatment.

In Fig. 31, the polarized light micrographs (PLM) indicate SAC105 had similar multiple grain structures as SACM for samples without thermal aging pretreatment. With thermal aging pretreatment, the number of grains of SAC105 degenerated into a reduced number, while that of SACM maintained the same. For SACC, only very few grains can be discerned for samples without thermal aging pretreatment. The low grain number feature was maintained with additional thermal aging pretreatment.

6. Mechanical Properties

The hardness of solder joints after TCT was determined, as shown in Fig. 33. Thermal aging prior to TCT caused the hardness of SAC105 joints to decrease. On the other hand, SACM was insensitive to this thermal aging pretreatment, and maintained the same hardness as the sample without thermal aging.

The tensile properties of several lead-free alloys were measured, as shown in Fig. 34. SAC305 exhibited the highest value in tensile strength, yield strength, Young's modulus, and elongation (%). SACM and SAC105 are fairly comparable, except that SACM is better than SAC105 in elongation.

DISCUSSION

1. TCT Performance

SACM and SACC showed a higher TCT reliability than that of SAC105. Both also compared favorably with SAC305, as shown in Fig. 12, 13, and 14. The high TCT reliability of SACM and SACC can be attributed to their high stability in microstructure, as shown in Fig. 31 and Fig. 32. Presence of Mn or Ce effectively suppressed the coarsening of IMC particles, thus maintained the hardness of solder joint. On the other hand, SAC105 displayed coarsening of IMC particles, and the resultant decrease in hardness of solder joints with increasing thermal aging, as shown in Fig. 33.

The greater TCT reliability may also be attributed to (1) finer



Figure 30: Intermetallic compounds at solder/TFBGA (NiAu) interface for solder bumps aged at 150°C (10,000X). Solder has been selectively removed by etching.



Figure 31: Effect of alloy type and thermal aging pretreatment prior to TCT on the microstructure of thermal cycled devices.

IMC texture at interface, and (2) thinner IMC layer. It has been reported that Co, Ni or Pt inclusion in 97Sn3Ag soldered onto Cu substrate did not coarsen IMC scallop size or increase IMC thickness and grain size significantly after 4 times solder reflow. This IMC suppression phenomenon was accomplished by having Co, Ni and Pt dissolved in IMC layer [7]. The grain size stability can be attributed to the pinning of grain boundary by the abundant fine IMC particles. In view of this, it is reasonable to speculate that the IMC suppression phenomenon observed in SACM and SACC was also resulted from inclusion of Mn or Ce in the IMC.

The coarsening of IMC particles should be responsible for the grain coarsening of SAC105, as shown in the polarized light micrographs in Fig. 31. Solder with coarsened grains in general tends to exhibit a higher creep rate [8] and consequently a poorer thermal fatigue life. In contrast, SACM showed no sign of grain coarsening. This phenomenon is consistent with the IMC and grain size suppression effect observed for Co, Ni and Pt.

However, the role of a fine grain structure in high TCT reliability should not be over emphasized. In Fig. 31, SACC showed a steady but coarse grain structure. And, as stated above, SACC joints are fairly high in TCT reliability. Thus, it can be concluded that a stable and fine IMC structure is the primary contributing factor, and a stable grain structure is the secondary cause for SACM and SACC to exhibit a high TCT reliability.

Drop Test Performance

Both JDT and DBT are tests designed to predict the resistance against drop failure for portable devices. By examining Fig 6, 7, and 26, the results of both methods indicate that SACM and SACC performed considerably better than SAC105 and SAC305. By



Figure 32: Microstructure of solder joints of TFBGA (NiAu) on PCB (OSP) after TCT.

examining Fig. 27-32, both SACM and SACC exhibit finer IMC structure at interface. Besides, SACM exhibits a thinner IMC layer, which has also been reported in previous studies [9, 10]. SACC showed a thinner IMC layer at PCB side.

Addition of small amount of certain additives not only suppresses the IMC growth and grain coarsening, but also causes low frequency of occurrence of IMC fracture in high impact pull test, and was very effective for improving drop test performance [7]. Presumably inclusion of these additives in the IMC layer reduced the brittleness of IMC structure. The findings in those studies help explaining the improved drop test performance of SACM and SACC.

2. CBT Performance

In CBT test, the reliability ranking was observed as: SAC305 >> SACC, SACM, SAC105 > SnPb. The superior performance of SAC305 can be attributed to it mechanical property, as shown in Fig. 34. Since all lead-free alloys showed a higher CBT reliability than the control SnPb, the relative performance of lead-free systems is considered non-consequential in terms of finding a valid lead-free alternative for SnPb.

3. Surface Finish

The relative performance of PCB surface finishes in the three tests JDT, TCT, and CBT is interestingly consistent: ImAg > OSP > ENIG.

On the other hand, the relative performance of TFBGA surface finishes is more complicated. In TCT, NiAu > OSP. In CBT, NiAu > OSP for as reflowed or thermally cycled samples. In JDT, for thermally cycled devices, NiAu > OSP. For as reflowed devices or thermally aged devices, OSP > NiAu.

All these results indicate that for thermally cycled devices the drop, cyclic bending and thermo-mechanical fatigue reliabilities with NiAu finished packages are higher than those with OSP finished packages. The reason for these may be due to the fact that the solder joints with asymmetric substrates (Cu:NiAu) have lower creep rates than those with symmetric substrates (Cu:Cu) [11]. In view of these reliability results in the present paper, NiAu should be a preferred surface finish for BGA packages if assembled in the popular OSP finished PCBs since all electronic devices experience temperature cycling in service.







Figure 34: Mechanical properties of SACM, SAC105, and SAC305.

CONCLUSION

The Mn or Ce doped low cost SAC105 alloys achieved a higher drop test and dynamic bending test reliability than SAC105 and SAC305, and exceeded SnPb for some test conditions. More significantly, being a slightly doped SAC105, both SACM and SACC matched SAC305 in thermal cycling performance. In other words, the low cost SACM and SACC achieved a better drop test performance than the low Ag SAC alloys plus the desired thermal cycling reliability of high Ag SAC alloys. The mechanism for high drop performance and high thermal cycling reliability can be attributed to a stabilized microstructure, with uniform distribution of fine IMC particles, presumably through the inclusion of Mn or Ce in the IMC. The cyclic bending results showed SAC305 being the best, and all lead-free alloys are equal or superior to SnPb. The reliability test results also show that NiAu is a preferred surface finish for BGA packages over OSP if assembled in the popular OSP finished PCBs.

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				JEDEC	Drop Te	est Weib	ull Plot	Data				
Alloy	150C/0 hr			150C/100 hrs		150C/250 hrs			250 TCT			
	β	η	ρ	β	η	ρ	β	η	ρ	β	η	ρ
SnPb	3.144	111	0.981	2.458	79.72	0.893	2.915	108.8	0.99	3.583	139.7	0.964
SAC105	1.429	197.3	0.972	1.079	61.76	0.919	1.002	34.24	0.95	1.345	120.9	0.952
SAC305	1.139	31.85	0.987	0.953	47.52	0.965	1.249	27.42	0.957	1.063	58.84	0.926
SACM	2.273	237.2	0.962	1.509	92.59	0.96	1.047	69.54	0.929	2.177	179.2	0.974
SACC	3.873	239.4	0.969	1.055	199.6	0.953	1.08	114.3	0.969	1.254	202.1	0.971
			1	Thermal	Cycle T	est Weil	bull Plot	Data				
Alloy	150C/0 hr			150C/100 hrs		150C/250 hrs						
	β	η	ρ	β	η	ρ	β	η	ρ			
SnPb	8.667	1305	0.967	7.743	1125	0.938	7.058	1112	0.944			
SAC105	3.409	1541	0.981	7.646	1388	0.941	7.943	1468	0.963			
SAC305	7.506	2154	0.968	8.35	1861	0.996	5.805	1906	0.965			
SACM	3.169	1706	0.974	7.22	1762	0.982	5.780	2034	0.946			
SACC	5.161	1809	0.898	5.66	1896	0.929	6.845	2385	0.966			
				Cyclic B	ending	Test Wei	bull Plot	Data				
Alleri	150C/0 hr			150C/100 hrs		150C/250 hrs			250 TCT			
Alloy	β	η	ρ	β	η	ρ	β	η	ρ	β	η	ρ
SnPb	3.077	4046	0.923	4.615	2940	0.979	3.452	2854	0.93	2.282	8610	0.927
SAC105	3.683	8592	0.973	5.032	4266	0.979	4.667	2991	0.988	3.936	3723	0.934
SAC305	1.67	65302	0.952	2.934	9811	0.987	3.042	6913	0.986	3.596	10367	0.979
SACM	3.426	9018	0.991	3.657	3807	0.973	3.326	1953	0.952	3.079	2190	0.96
SACC	3.038	8634	0.975	2.155	3071	0.96	3.755	2164	0.959	1.481	1589	0.94

Appendix 1: Weibull data for JDT, TCT, and CBT.

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Metal Etching Technology Lumberton, NJ

Micro Care Corporation New Britain, CT

Micro Industries Westerville, OH

Micro Systems Engineering Inc. Lake Oswego, OR

Micromeritics Instrument Corporation Norcross, GA

MicroScreen South Bend, IN Microstructures, Inc. Ham Lake, MN

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Millennium Electronics, Inc Crystal Lake, IL

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Multi-Fineline Electronix Anaheim, CA

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NAMC - Not Another Marketing Company Belmar, NJ

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NEA Inc. Londonderry, NH

New Wave Components Eden Prairie, MN

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Nu-Way Electronics, Inc. Elk Grove Village, IL

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OnCore Manufacturing Services LLC San Marcos, CA

Orpro Vision Billerica, MA P. Kay Metal, Inc. Los Angeles, CA

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